1.1.2: The Institution adheres to the academic calendar including for the conduct of continuous internal evaluation (CIE).

CONTENTS

PRINCIPAL
S.J.M.I.T, CHITRADURGA

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NH-4 Bypass, P.B.No:73, CHITRADURGA -577502, Karnataka State

Department: Electronics & Communication				Name of the faculty: Nandini G R	
Course Title: Introduction to Electronics & Communication				Course Code :BESCK104C	
Semester :I	Section: A& B	Test: I	Date :31/10/2023	Time :2:45- 3:45	Max. Marks :25
Note:*Answer any TWO full questions*					

Q.No.	QUESTIONS	Marks	CL	CO	PO
1.a)	Draw the block diagram of DC power supply and explain the individual blocks.	6.5	U	22C104.1	1,6
1.b)	Determine: i) The voltage gain ii) The current gain iii) The power gain. An amplifier produces an output voltage of 2V for an input of 50mV. If the input and output currents in this condition are 4mA and 200mA respectively.	6	Ap	22C104.1	1,2,5,6
	OR				
2.a)	Draw the circuit diagram of voltage regulation and explain the operation.	6.5	U	22C104.1	1,2,3 ,5
2.b)	Describe the working of a capacitor filter for a half wave rectifier with a neat circuit diagram and necessary waveforms.	6	U	22C104.1	2,5
3.a)	With a neat circuit diagram and waveform. Explain the working operation of a full wave rectifier.	6.5	U	22C104.1	1,2,3 ,6
3.b)	Discuss briefly a negative feedback amplifier with block diagram and Derive for Voltage gain.	6	U	22C104.1	1,2,3 ,5
	OR				
4.a)	With a neat circuit diagram and waveform. Explain the working operation of a full wave bridge rectifier.	6.5	U	22C104.1	1,2,3 ,6
4.b)	Determine a suitable value of series resistor for operation in conjunction with a supply of 9V.A 5V zener diode has a maximum rated power dissipation of 500 mW. If the diode is to be used in a simple regulator circuit to supply a regulated 5V to a load having a resistance of 400 Ω,	6	Ap	22C104.1	1,2,3 ,5

(CL) CognitiveLevel

(R): Remembering, **(U)**:Understanding,**(Ap)**: Apply, **(A)**:Analysis, **(E)**: Evaluation, **(C)**: Creation.

COURSE OUTCOMES (COs) COVERED

CO1: Describe the concepts of electronic circuits encompassing power supplies and amplifiers.

Academic Coordinator
(Prof.Nandini G R)

H.O.D
(Dr.Siddesh K.B)

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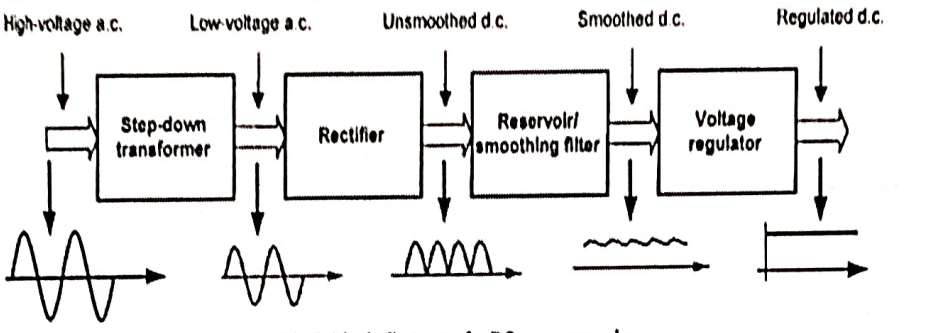
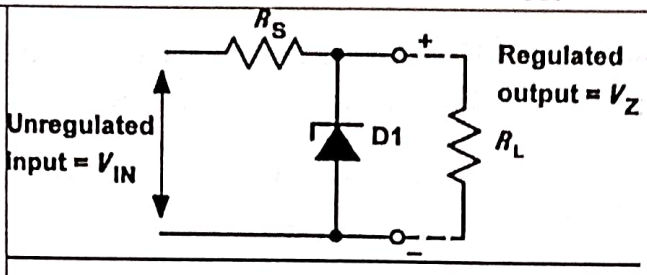
Scheme of Evaluation: Internal Assessment – 1

Department: Electronics & Communication				Name of the faculty: Nandini G R	
Course Title: Introduction to Electronics & Communication				Course Code : BESCK104C	
Semester : 1	Section: A& B	Test: 1	Date : 31/10/2023	Time : 2:45-3:45	Max. Marks : 25

Q.No.	QUESTIONS	Marks
1.a)	 Fig.1. Block diagram of a DC power supply **Step down transformer:** It is a device that has two coil windings: primary and secondary used to convert a high AC voltage (230V/ 50Hz) to a required low AC voltage. **Rectifier:** It is a device has one or more diodes, converts secondary AC voltage to pulsating DC. **Smoothening Filter:** It is a circuit used to remove fluctuations (ripple or ac) present in rectifier output. Example: Capacitor filters, LC filters, π- filters, etc.. **Voltage Regulator:** Voltage regulator is a circuit which provides constant DC output voltage irrespective of changes in load current or changes in input voltage.	2.5M 4M
1.b)	(a) The voltage gain is calculated from: $A_v = \frac{V_{out}}{V_{in}} = \frac{2\ V}{50\ mV} = 40$ (b) The current gain is calculated from: $A_i = \frac{I_{out}}{I_{in}} = \frac{200\ mA}{4\ mA} = 50$ (c) The power gain is calculated from: $A_p = \frac{I_{out} \times V_{out}}{I_{in} \times V_{in}} = \frac{200\ mA \times 2\ V}{4\ mA \times 50\ mV} = \frac{0.4\ W}{200\ \mu W} = 2,000$ Note that the same result is obtained from: $A_p = A_i \times A_v = 50 \times 40 = 2,000$	2M 2M 2M

OR

2.a)



2.5

- The series resistor, *RS* is connected in the circuit to limit the current through the zener diode to a safe value when load *RL* is disconnected. Also, the voltage drop across it is a part of unregulated input voltage, *Vin*. When *RL* is connected, zener current *IZ* will reduce as current ($I = Iz + IL$) is split into load *RL*. Output voltage VO, remains constant until regulation fails. Regulation fails at a point at which potential divider formed by *RS* and *RL* produces lower voltage than VZ voltage.

$$V_Z = V_{IN} \times \frac{R_L}{R_L + R_S}$$

- where *VIN* is the unregulated input voltage. Thus the *maximum* value for *RS* can be calculated from:

$$R_{Smax} = R_L \times \left(\frac{V_{IN}}{V_Z} - 1\right)$$

4M

The power dissipated in the zener diode will be given by $PZ = IZ \times VZ$, hence the minimum value for *RS* can be determined from the off-load condition when:

$$R_{Smin} = \frac{(V_{IN}V_Z) - V_Z^2}{P_{Zmax}}$$

where P_Z max is the maximum rated power dissipation for the zener diode.

2.b)

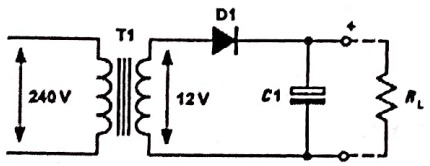
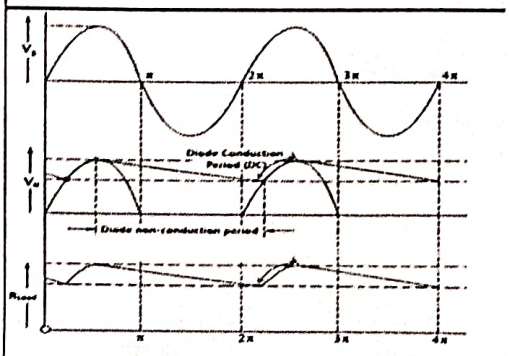
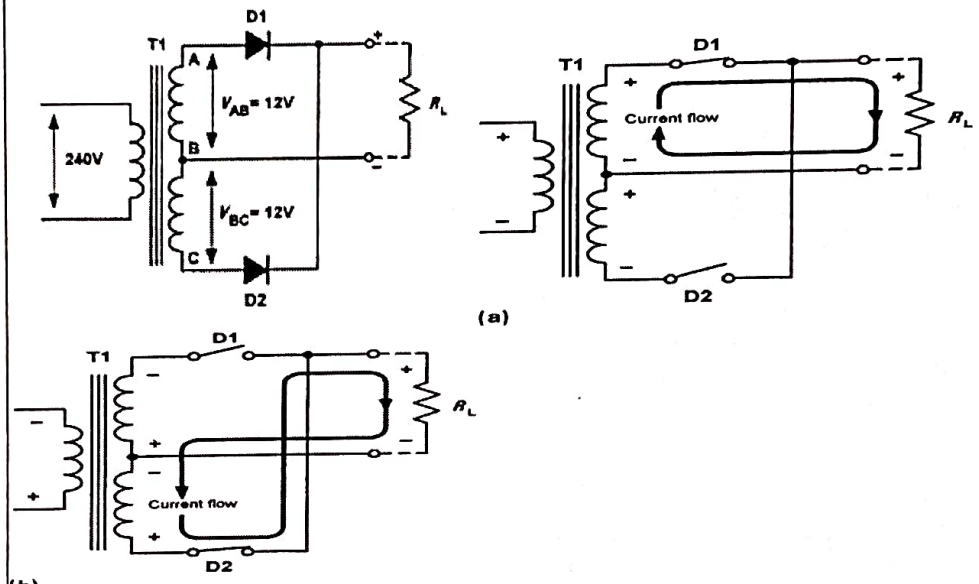
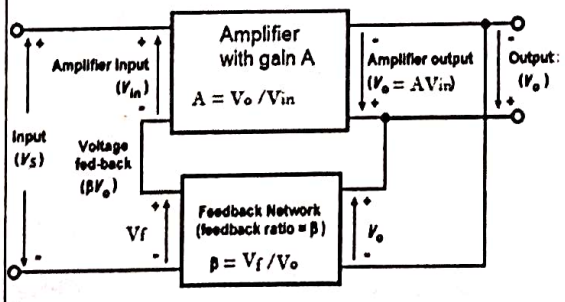


Figure 6.6 A simple half-wave rectifier circuit with reservoir capacitor

2M



	• Charging Time of C1 to the peak value = Rseries x C1 $R_{series} = R_{secondary\ winding} + R_{diode} + R_{wiring\ and\ connections}$ Hence C1 charges quickly as soon as diode conducts. • Discharging Time of C1 = R_L x C1 Practically, RL is very much larger than Rseries Hence C1 discharges slowly through R_L. Explanation.....	4M
3.a)	 Explanation.....	2.5M 4M
3.b)		2M

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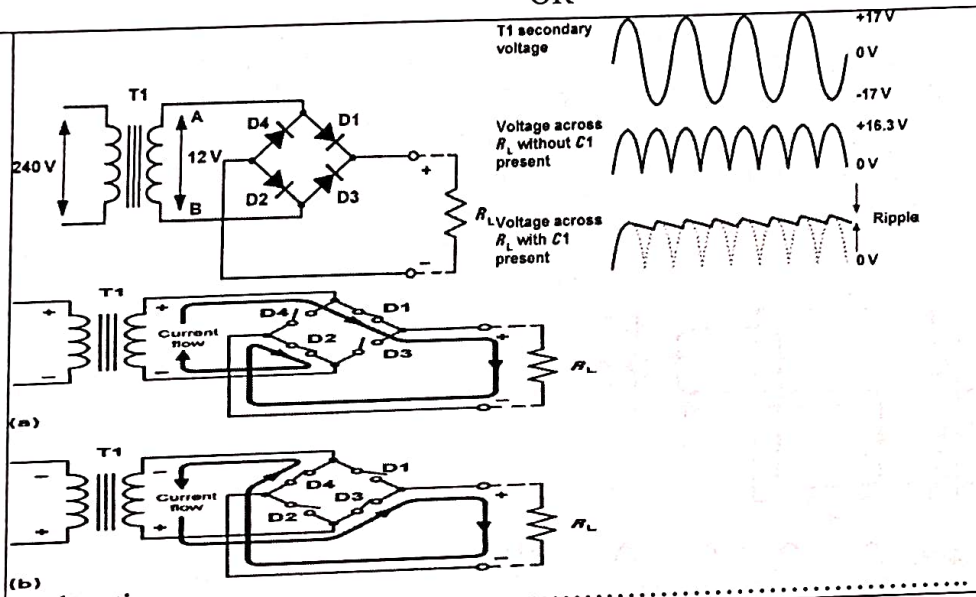
	$A = Vo/V_{in}$ $Vo = A\ V_{in}$. where $V_{in} = V_S - V_f$ and $V_f = \beta Vo$ $Vo = A(Vs - \beta Vo)$ $Vo = AVs - A\beta Vo$ $Vo + A\beta Vo = AVs$ $AVs = Vo\ (1 + A\beta)$ So, the equation of overall gain with negative feedback is given by $\frac{V_o}{V_s} = A_f = \frac{A}{1 + A\beta}$	4M
	OR	
4.a)	 Explanation.....	2.5M 4M
4.b)	R_S max. $= R_L \times \left(\frac{V_{in}}{V_{in}} - 1\right)$ thus: R_S max. $= 400 \times \left(\frac{9}{5} - 1\right) = 400 \times (1.8 - 1) = 320\ \Omega$ Now we need to determine the minimum value for the series resistor, R_S: R_S min. $= \frac{V_{in}V_Z - V_Z^2}{P_Z \text{ max.}}$ thus: R_S min. $= \frac{(9 \times 5) - 5^2}{0.5} = \frac{45 - 25}{0.5} = 40\ \Omega$ Hence a suitable value for R_S would be 150 Ω (roughly mid-way between the two extremes).	3M 3M

Academic Coordinator
(Prof.Nandini G R)

H.O.D
(Dr.Siddesh K.B)

Head of the Dept.
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CHITRADURGA - 577502.

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First Internals Attendance

Name of the Faculty: NANDINI. G.R	Department: ELECTRONICS & COMMUNICATION	
Subject Name: INTRODUCTION TO ELECTRONICS & COMMUNICATION	Semester : 1st	Section: A
Subject Code: BESCK104C	Date : 31/10/2023	Time: 2:45 - 3:45

Sl No	BRANCH	NAME OF THE STUDENT	Signature
1.	CS	ABHINAIK N	
2.	CS	ABHISHEK L	
3.	CS	AISHA ABDUL SHUKOOR	
4.	CS	AKARSHA SAJJAN B	
5.	CS	AKASH G	
6.	CS	AMITH PATIL	
7.	CS	AMITH V	
8.	CS	AMRUTHA C M	
9.	CS	ANKITHA J	
10.	CS	ANUSHA R H	
11.	CS	ANUSHREE P M	
12.	CS	ARPITHA R	
13.	CS	BHAVANASHREE S	
14.	CS	CHAITRA B	
15.	CS	CHAITRA JAGADISH BADEGONDRA	
16.	CS	CHAITRA SURESH ARIKATTE	
17.	CS	CHANDANA S R	
18.	CS	CHANDANA V	
19.	CS	CHIDANANDA G	
20.	CS	CHINMAYEE U	
21.	CS	CHINMAYI M K	
22.	CS	DARSHAN B S	
23.	CS	DARSHAN G P	
24.	CS	DARSHITHA G P	
25.	CS	DHANUSH H	
26.	CS	DILIP M P	
27.	CS	DIVYA U	
28.	CS	G R GOWRI	
29.	CS	GANESH C Y S	
30.	CS	GANESH M M	
31.	CS	GHOUSIYA FATHIMA A	
32.	CS	GIRISH KUMAR M	
33.	CS	GIRISH PARAGOND KAMATAGI	
34.	CS	GULAM HUSSAIN	
35.	CS	HRUTHIK S	

36.	CS	JAYANTH S P	
37.	CS	JEEVAN R	
38.	CS	K S KISHAN	
39.	CS	KARTHIK E HALAGERI	
40.	CS	KARTHIK J	
41.	CS	KAVANA K	
42.	CS	KIRAN JADADARI	
43.	CS	KUSUMA M	
44.	CS	LAKSHMANA N	
45.	CS	MADHURA G M	
46.	CS	MANUSHREE M	
47.	CS	MEGHA MANJAPPA MOGALI	
48.	CS	MEGHANA A B	
49.	CS	MEGHANA G S	
50.	CS	MINAL R S GOWDA	
51.	CS	MOHAMAD MUTHAWAKAL G	
52.	CS	MOHAMED GHOUSE	
53.	CS	MOHAMMED SHAFIQ	
54.	CS	MOHAMMED SHREYAN	
55.	CS	MUBARAK PASHA	
56.	CS	MUTHU RAJ J R	
57.	CS	NAGARAJ G R	
58.	CS	NANDINI G R	
59.	CS	PRAVALIKA	
60.	CS	T M RITHIN	
61.	CS	V TEJASWINI	
62.	CS	YUVARAJ D	
63.	CS	SUHA FATHIMA M J	

Total Number of Students Present:	63
Number of Students Absent:	00
Total Number of Students:	63
Name & Signature of Invigilator	
Name & Signature of Subject In-Charge	31/10/23

Prof.Madhu.K.C
First Year Coordinator

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Department: Electronics & Communication Engineering				Name of the faculty: Nandini G R	
Course Title: Introduction to Electronics & Communication				Course Code : BESCK104C	
Semester : I	Section: A& B	Test: II	Date : 05/12/2023	Time : 2:45- 3:45	Max. Marks : 25
Note: *Answer any **TWO** full questions*					

Q.No.	QUESTIONS	Marks	CL	CO	PO	PSO
1.a)	Explain the operation of three- stage ladder RC Network Oscillator with neat circuit diagram.	6.5	U	22C104.2	1,2,3,5	-
1.b)	Explain a differentiator circuit with waveforms and circuit diagrams.	6	U	22C104.2	1,3,5,6	-
	OR					
2.a)	(i)Determine the frequency of oscillations of a 3-stage ladder network oscillator in which C=10nF and R= 10kΩ. (ii) Explain the Barkhausen criteria for Oscillations. In wein bridge oscillator if C1=C2=100nF, determine the frequency of oscillations when R1=R2=1kΩ	6.5	Ap	22C104.2	1,2, 3,5	-
2.b)	What are the characteristics of an ideal operational amplifier?	6	U	22C104.2	1,2, 3,5	-
3.a)	Implement full adder circuit with its truth table and write the expressions for sum and carry.	6.5	Ap	22C104.3	1,3, 5,9	-
3.b)	State and prove De-Morgan's theorems with its truth table.	6	U	22C104.3	1,3, 5,9	-
	OR					
4.a)	Express the Boolean function F= A+ $\bar{B}C$ in a sum of minterms form.	6.5	Ap	22C104.3	1,3, 5,9	-
4.b)	Perform the following operations: (i) 1010100-1000100 using 2's complement method. (ii) 4456-34234 using 9's complement method. (iii) 4456-34234 using 10's complement method.	6	Ap	22C104.3	1,2, 3,5	-

(CL) Cognitive Level

(R): Remembering, **(U)**:Understanding,**(Ap)**: Apply, **(A)**:Analysis, **(E)**: Evaluation, **(C)**: Creation.

COURSE OUTCOMES (COs) COVERED

22C104.1: Describe the concepts of electronic circuits encompassing power supplies and amplifiers.

22C104.2: Describe the concepts of Oscillators and Operational amplifiers.

22C104.3: Develop competence knowledge to construct basic digital circuits by make use of basic gate and its function.

22C104.4: Discuss the characteristics and technological advances of embedded systems.

22C104.5 Explain the different modes of communication from wired to wireless and the computing involved

Academic Coordinator
(Prof.Nandini G R)

H.O.D
(Dr.Siddesh K.B)

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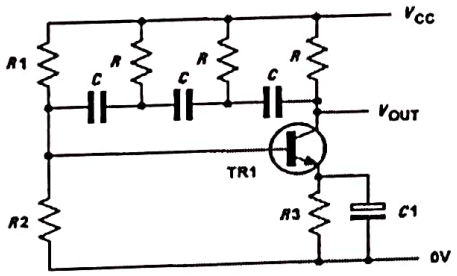
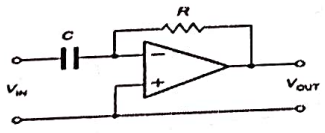
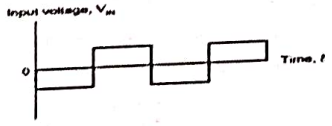
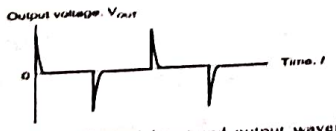
Scheme of Evaluation: Internal Assessment – II

Department: Electronics & Communication Engineering				**Name of the faculty: Nandini G R**	
Course Title: Introduction to Electronics & Communication				**Course Code : BESCK104C**	
Semester : I	**Section: A& B**	**Test: II**	**Date : 05/12/2023**	**Time : 2:45-3:45**	**Max. Marks : 25**

Q.No.	QUESTIONS	Marks
1.a)	 $f = \frac{1}{2\pi \times \sqrt{6}CR}$ A simple phase-shift oscillator based on a three stage C–R ladder network is shown in Figure TR1 operates as a conventional common-emitter amplifier stage with **R1 and R2 providing base bias potential** and **R3 and C1 providing emitter stabilization**. The total phase shift provided by the C–R ladder network (connected between collector and base) is 180° at the frequency of oscillation. The transistor provides the other 180° phase shift in order to realize an overall phase shift of 360° or 0°.	3.5M 3M
1.b)	 Figure 8.13 A differentiator   Figure 8.14 Typical input and output waveforms for a differentiator A differentiator produces an output voltage that is equivalent to the rate of change of its input.An op-amp differentiator is an inverting amplifier, which uses a capacitor C in series with the input voltage V_{in} and a feedback resistor R is connected between V_{out} and inverting (-) input.	2M 2M 2M

OR

2.a) a)

Solution

Using

$$f = \frac{1}{2\pi \times \sqrt{6}CR}$$

gives

$$f = \frac{1}{6.28 \times 2.45 \times 10 \times 10^{-9} \times 10 \times 10^{3}}$$

from which

$$f = \frac{1}{6.28 \times 2.45 \times 10^{-4}} = \frac{10^{4}}{15.386} = 647 \text{ Hz}$$

3M

b)

(a) the feedback must be positive
(i.e. the phase shift must be 0° or 360°.);
(b) the overall loop voltage gain must be greater than 1

1M

When $R1 = R2 = 1\ k\Omega$

$$f = \frac{1}{2\pi CR}$$

where $R = R1 = R1$ and $C = C1 = C2$.

Thus

$$f = \frac{1}{6.28 \times 100 \times 10^{-9} \times 1 \times 10^{3}}$$

$$f = \frac{10^{4}}{6.28} = 1.59 \text{ kHz}$$

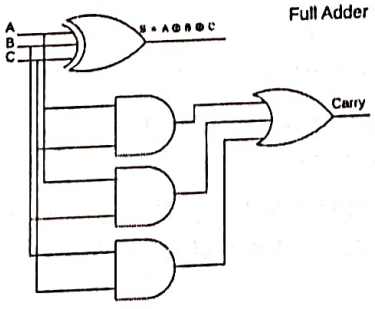
2.5M

2.b) Characteristics for an 'ideal' operational amplifier are:
(a) The open-loop voltage gain should be very high (ideally infinite).
(b) The input resistance should be very high (ideally infinite).
(c) The output resistance should be very low (ideally zero).
(d) Full-power bandwidth should be as wide as possible (ideally infinite).
(e) Slew rate should be as large as possible (ideally infinite).
(f) Input offset should be as small as possible (ideally zero).

6M

3.a) Truth Table

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Full Adder

Sum = A⊕B⊕C
Carry = AB + BC + CA] Derivation

3M

3.5M

3.b) — 4M

1) $(x+y)' = x' \cdot y'$

x	y	x+y	(x+y)'	x'	y'	x'.y'
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

2) $(xy)' = x' + y'$

x	y	xy	(xy)'	x'	y'	x'+y'
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

Statement..... — 2M

4.a) — 3.5M + 3M

$F = A + \bar{B}C$

$A = A(B + \bar{B}) = AB + A\bar{B}$

$AB + A\bar{B} = ABC(C + \bar{C}) + A\bar{B}(C + \bar{C})$

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C}$

$\bar{B}C = BC(A + \bar{A})$

$= ABC + \bar{A}BC$

$F = ABC + \bar{A}BC + AB\bar{C} + A\bar{B}C + AB\bar{C}$

$= \bar{A}BC + AB\bar{C} + A\bar{B}C + AB\bar{C} + ABC$

$= m_1 + m_4 + m_5 + m_6 + m_7$

$F(A, B, C) = \Sigma(1, 4, 5, 6, 7)$

4.b) — 2M + 2M + 2M

i) 1010100 + 0111100 → 2's complement

(1) 0010000

Discard carry

Ans: $(0010000)_2$

ii) using 9's 8 complement

04456 + 65765 → 9's complement

70221

99999 − 70221

29778

Ans: $-(29778)_{10}$

iii) 04456 + 65766 = 70222

99999 − 70222 = 29777 + 1 = (29778)

29778

Ans: $-(29778)_{10}$

Academic Coordinator
(Prof.Nandini G R)

H.O.D
(Dr.Siddesh K.B)

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Second Internals Attendance

Name of the Faculty: NANDINI G R	Department: E&CE	
Subject Name: INTRODUCTION TO ELECTRONICS AND COMMUNICATION	Semester : 1st	Section: A
Subject Code: BCSCK104C	Date : 05/12/2023	Time: 2:45 - 3:45

Sl No	BRANCH	NAME OF THE STUDENT	Signature
1.	CS	ABHINAIK N	
2.	CS	ABHISHEK L	
3.	CS	AISHA ABDUL SHUKOOR	
4.	CS	AKARSHA SAJJAN B	
5.	CS	AKASH G	
6.	CS	AMITH PATIL	
7.	CS	AMITH V	
8.	CS	AMRUTHA C M	
9.	CS	ANKITHA J	
10.	CS	ANUSHA R H	
11.	CS	ANUSHREE P M	
12.	CS	ARPITHA R	
13.	CS	BHAVANASHREE S	
14.	CS	CHAITRA B	
15.	CS	CHAITRA JAGADISH BADEGONDRA	
16.	CS	CHAITRA SURESH ARIKATTE	
17.	CS	CHANDANA S R	
18.	CS	CHANDANA V	
19.	CS	CHIDANANDA G	
20.	CS	CHINMAYEE U	
21.	CS	CHINMAYI M K	
22.	CS	DARSHAN B S	
23.	CS	DARSHAN G P	
24.	CS	DARSHITHA G P	
25.	CS	DHANUSH H	
26.	CS	DILIP M P	
27.	CS	DIVYA U	
28.	CS	G R GOWRI	
29.	CS	GANESH C Y S	
30.	CS	GANESH M M	
31.	CS	GHOUSIYA FATHIMA A	
32.	CS	GIRISH KUMAR M	
33.	CS	GIRISH PARAGOND KAMATAGI	
34.	CS	GULAM HUSSAIN	
35.	CS	HRUTHIK S	

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36.	CS	JAYANTH S P	
37.	CS	JEEVAN R	
38.	CS	K S KISHAN	
39.	CS	KARTHIK E HALAGERI	
40.	CS	KARTHIK J	
41.	CS	KAVANA K	
42.	CS	KIRAN JADADARI	
43.	CS	KUSUMA M	
44.	CS	LAKSHMANA N	
45.	CS	MADHURA G M	
46.	CS	MANUSHREE M	
47.	CS	MEGHA MANJAPPA MOGALI	
48.	CS	MEGHANA A B	
49.	CS	MEGHANA G S	
50.	CS	MINAL R S GOWDA	
51.	CS	MOHAMAD MUTHAWAKAL G	
52.	CS	MOHAMED GHOUSE	
53.	CS	MOHAMMED SHAFIQ	
54.	CS	MOHAMMED SHREYAN	
55.	CS	MUBARAK PASHA	
56.	CS	MUTHU RAJ J R	
57.	CS	NAGARAJ G R	
58.	CS	NANDINI G R	
59.	CS	PRAVALIKA	
60.	CS	T M RITHIN	
61.	CS	V TEJASWINI	
62.	CS	YUVARAJ D	
63.	CS	SUHA FATHIMA M J	

Total Number of Students Present:	63
Number of Students Absent:	00
Total Number of Students:	63
Name & Signature of Invigilator	Uman. A.L. A.R
Name & Signature of Subject In-Charge	Nandini. G.R

Prof.Madhu.K.C
First Year Coordinator

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Department: Electronics & Communication Engineering				Name of the faculty: Nandini G R	
Course Title: Introduction to Electronics & Communication				Course Code : BESCK104C	
Semester : I	Section: A& B	Test: III	Date : 11/01/2024	Time : 2:45- 3:45	Max. Marks : 25
Note: *Answer any TWO full questions*					

Q.No.	QUESTIONS	Marks	CL	CO	PO
1.a)	Compare Embedded system with general computer systems.	6.5	U	22C104.4	1,6,9,12
1.b)	What is the difference between RISC and CISC processors?	6	R	22C104.4	1,6,9,12
	OR				
2.a)	Explain the working of a 7 segment LED with necessary diagrams.	6.5	U	22C104.4	1,2,3 ,5
2.b)	Explain Instrumentation and Control system with suitable diagrams.	6	U	22C104.4	1,2,3 ,5
3.a)	Describe the blocks of Modern Communication System with neat block diagram.	6.5	U	22C104.5	1,6,9 ,12
3.b)	Explain Amplitude Modulation (AM), Frequency Modulation (FM) and Phase Modulation (PM) with necessary waveforms.	6	U	22C104.5	1,2,3 ,5
	OR				
4.a)	Explain with a neat diagram, the concept of Radio wave propagation and its different types.	6.5	U	22C104.5	1,5,9 ,12
4.b)	Explain the following with the help of waveforms: (i) ASK (ii) FSK (iii) PSK	6	U	22C104.5	1,2,3 ,5

(CL) Cognitive Level

(R): Remembering, **(U)**:Understanding,**(Ap)**: Apply, **(A)**:Analysis, **(E)**: Evaluation, **(C)**: Creation.

COURSE OUTCOMES (COs) COVERED

22C104.1: Describe the concepts of electronic circuits encompassing power supplies and amplifiers.

22C104.2: Describe the concepts of Oscillators and Operational amplifiers.

22C104.3: Develop competence knowledge to construct basic digital circuits by make use of basic gate and its function.

22C104.4: Discuss the characteristics and technological advances of embedded systems.

22C104.5 Explain the different modes of communication from wired to wireless and the computing involved

Academic Coordinator
(Prof.Nandini G R)

H.O.D
(Dr.Siddesh K.B)

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Scheme of Evaluation: Internal Assessment – III

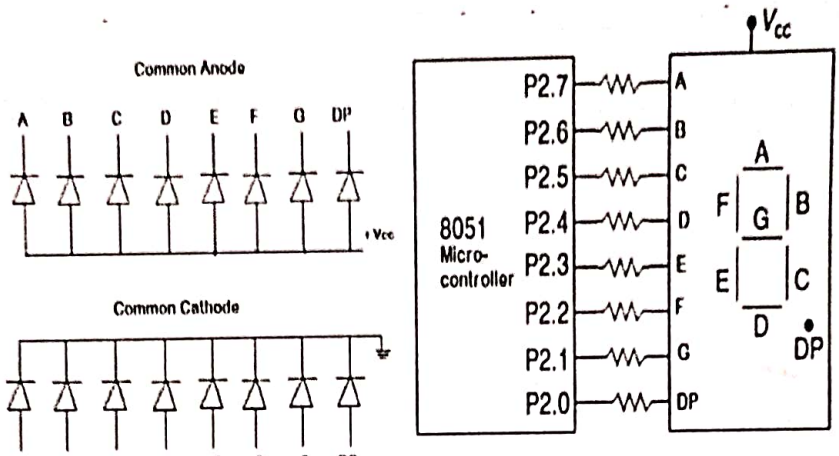
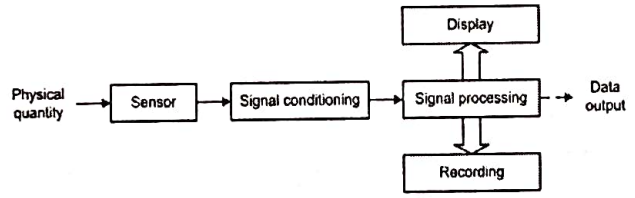
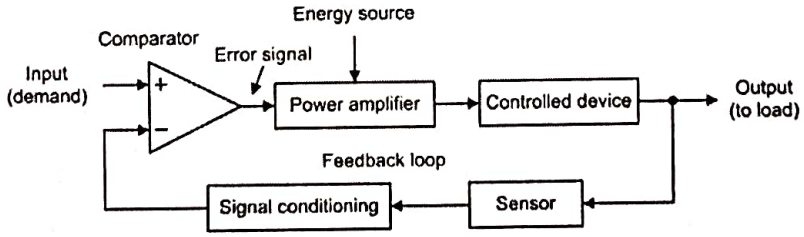
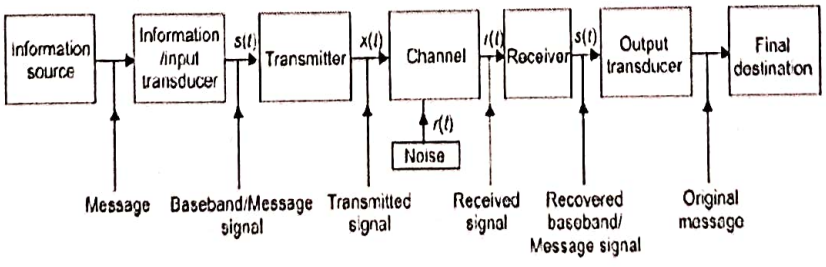
Department: Electronics & Communication Engineering				Name of the faculty: Nandini G R	
Course Title: Introduction to Electronics & Communication				Course Code :BESCK104C	
Semester : I	Section: A& B	Test: III	Date :11/01/2024	Time :2:45-3:45	Max. Marks :25

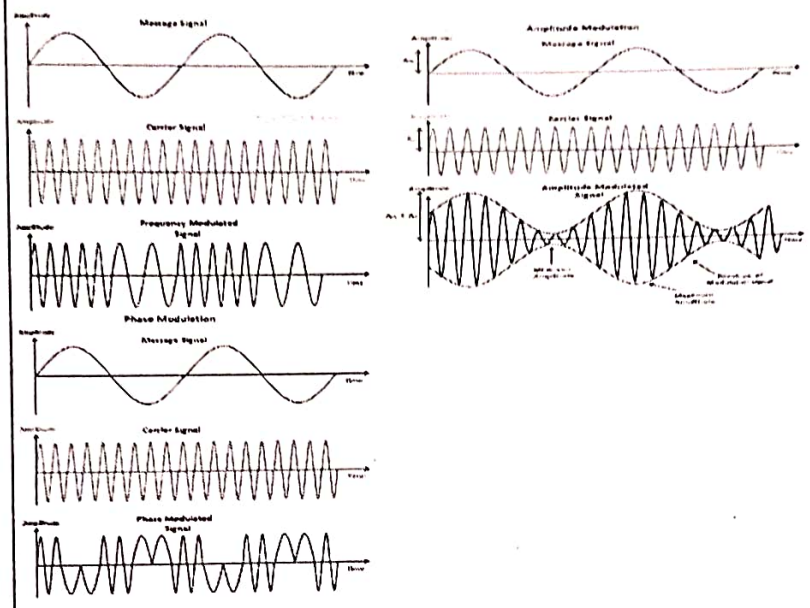
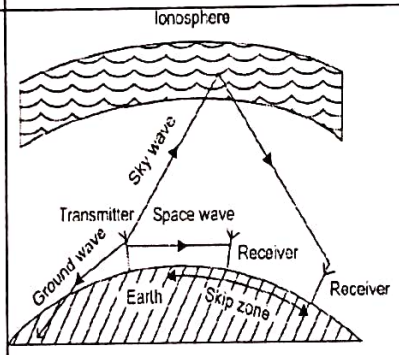
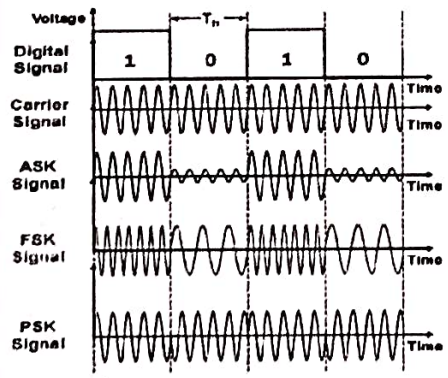
Q.No.	QUESTIONS	Marks
1.a)		6.5M

General Computing System	Embedded Systems
A system which is a combination of a generic hardware and general-purpose operating system for executing a variety of applications	A system which is a combination of a special-purpose hardware and embedded OS for executing a variety of applications
It contains a general-purpose operating system (GPOS)	It may or may not contain an operating system for functioning
Applications are alterable (programmable) by the user. (It is possible for end user to re-install the OS and also add or remove user applications)	The firmware of the Embedded system is pre-programmed and it is non-alterable by the end user.
It has 2 parts: Hardware and Software.	It has 3 parts: Hardware, Firmware and Software.
It can perform many tasks.	It performs specific tasks
Power consumption is high	Power consumption is less
Computers are usually bigger in size with larger hardware and input output devices attached to it	Embedded Devices are smaller in size than Computers, with limited hardware.

1.b) 6M

RISC	CISC
Reduced Instruction Set Computer.	Complex Instruction Set Computer.
Software centric design.	Hardware centric design.
Low power consumption.	High power consumption
Requires more RAM	Requires a minimum amount of RAM
Simple decoding of instruction.	Complex decoding of instruction.
Execution time is very less	Execution time is very high
It does not require external memory for calculations	It requires external memory for calculations
RISC architecture can be used with high-end applications like telecommunication, image processing, video processing, etc.	CISC architecture can be used with low-end applications like home automation, security system, consumer goods etc.
Fixed Instruction format (32-bit)	Varying formats (16 to 64 bits for each instruction)

2.a)	 Fig.4 7-segment LED interfacing with microcontroller Explanation.....	3M 3.5M
2.b)	 Fig. 1 Instrumentation system  Fig.2 shows the arrangement of a control system Explanation.....	3M 3M
3.a)	 Explanation.....	3M 3.5M

3.b)	 Explanation.....	3M 3M
4.a)	 Explanation.....	3M 3.5M
4.b)	 Explanation.....	3M 3.5M

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H.O.D
(Dr.Siddesh K.B)

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Third Internals Attendance

Name of the Faculty: NANDINI G R	**Department:** E & CE	
Subject Name: Introduction to Electronic Communication	**Semester : 1st**	**Section: A**
Subject Code: BESCK104C	**Date :** 11/01/2024	**Time:** 2:45 – 3:45

Sl No	BRANCH	NAME OF THE STUDENT	Signature
1.	CS	ABHINAIK N	
2.	CS	ABHISHEK L	
3.	CS	AISHA ABDUL SHUKOOR	
4.	CS	AKARSHA SAJJAN B	
5.	CS	AKASH G	
6.	CS	AMITH PATIL	
7.	CS	AMITH V	
8.	CS	AMRUTHA C M	
9.	CS	ANKITHA J	
10.	CS	ANUSHA R H	
11.	CS	ANUSHREE P M	
12.	CS	ARPITHA R	
13.	CS	BHAVANASHREE S	
14.	CS	CHAITRA B	
15.	CS	CHAITRA JAGADISH BADEGONDRA	
16.	CS	CHAITRA SURESH ARIKATTE	
17.	CS	CHANDANA S R	
18.	CS	CHANDANA V	
19.	CS	CHIDANANDA G	
20.	CS	CHINMAYEE U	
21.	CS	CHINMAYI M K	
22.	CS	DARSHAN B S	
23.	CS	DARSHAN G P	
24.	CS	DARSHITHA G P	
25.	CS	DHANUSH H	
26.	CS	DILIP M P	
27.	CS	DIVYA U	
28.	CS	G R GOWRI	
29.	CS	GANESH C Y S	
30.	CS	GANESH M M	
31.	CS	GHOUSIYA FATHIMA A	
32.	CS	GIRISH KUMAR M	
33.	CS	GIRISH PARAGOND KAMATAGI	
34.	CS	GULAM HUSSAIN	
35.	CS	HRUTHIK S	

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36.	CS	JAYANTH S P	Jayanth
37.	CS	JEEVAN R	
38.	CS	K S KISHAN	K.S. Kishan
39.	CS	KARTHIK E HALAGERI	
40.	CS	KARTHIK J	
41.	CS	KAVANA K	Kavana. K.
42.	CS	KIRAN JADADARI	
43.	CS	KUSUMA M	Kusuma. M
44.	CS	LAKSHMANA N	Laxmana
45.	CS	MADHURA G M	Madhura GM
46.	CS	MANUSHREE M	Manushree. M
47.	CS	MEGHA MANJAPPA MOGALI	
48.	CS	MEGHANA A B	Meghana AB
49.	CS	MEGHANA G S	Meghana. G.S
50.	CS	MINAL R S GOWDA	Minal. R S. Gowda
51.	CS	MOHAMAD MUTHAWAKAL G	Muthakal
52.	CS	MOHAMED GHOUSE	Md Ghouse
53.	CS	MOHAMMED SHAFIQ	Mdshafiq
54.	CS	MOHAMMED SHREYAN	Recommended Shreyan
55.	CS	MUBARAK PASHA	Mubarak
56.	CS	MUTHU RAJ J R	Muthu Raj
57.	CS	NAGARAJ G R	Nagaraj. G R
58.	CS	NANDINI G R	Nandu
59.	CS	PRAVALIKA	Pravalika.
60.	CS	T M RITHIN	Rithin
61.	CS	V TEJASWINI	V. Tejaswini.
62.	CS	YUVARAJ D	Yuvaraj. D
63.	CS	SUHA FATHIMA M J	Suha FM. J

Total Number of Students Present:	63
Number of Students Absent:	00
Total Number of Students:	63
Name & Signature of Invigilator	Pradeep Kumar. V
Name & Signature of Subject In-Charge	Nandini GR 11/12/24

Prof.Madhu.K.C
First Year Coordinator

CBCS SCHEME

USN | | | | | | | | | | |

BESCK104C/BESCKC104

First Semester B.E./B.Tech. Degree Examination, June/July 2023
Introduction to Electronics and Communication

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.
3. Assume any missing data suitably.

		Module – 1	M	L	C
Q.1	a.	Describe the DC power supply with the help of block diagram.	7	L2	CO1
	b.	Explain Full-wave Rectifier with necessary circuit diagrams and waveforms.	8	L2	CO1
	c.	Describe the terms : Gain, Input Resistance, Band width of Amplifier.	5	L2	CO1
		OR			
Q.2	a.	Describe Half-wave rectifier with circuit diagrams and waveforms.	8	L2	CO1
	b.	Classify different types of Amplifier.	8	L2	CO1
	c.	An amplifier produces an output voltage of 2V for an input of 50 mV. If the input and output currents are 4 mA and 200 mA respectively, determine (i) The voltage gain (ii) The current gain (iii) The power gain.	4	L3	CO1
		Module – 2			
Q.3	a.	What are characteristics of an ideal operational amplifier?	6	L2	CO2
	b.	Explain a differentiator circuit with waveforms and circuit diagrams.	7	L2	CO2
	c.	Describe wein bridge oscillator with circuit diagram and formulas for frequency of oscillations.	7	L2	CO2
		OR			
Q.4	a.	Explain the following terms with reference to Operational Amplifiers. (i) Open loop voltage gain (ii) Input Resistance (iii) Input offset voltage (iv) Slew Rate	8	L2	CO2
	b.	Describe three basic configurations for operational Amplifiers.	8	L2	CO2
	c.	Determine the frequency of oscillations of a 3-stage ladder network oscillator in which C = 10 nF and R = 10 kΩ .	4	L3	CO2
		Module – 3			
Q.5	a.	Perform the following operations: (i) 1101 – 0101 using 2's complement method (ii) 0110 – 0010 using 2's complement method (iii) 924 – 126 using 9's complement method (iv) 265 – 424 using 10's complement method	8	L3	CO3
	b.	Simplify the following expressions using Boolean algebra: (i) $\bar{A}BC + AB\bar{C} + AB$ (ii) $A + BC + B$	7	L3	CO3
	c.	Design a Half Adder circuit with necessary logic diagram and expressions.	5	L2	CO3
		OR			
Q.6	a.	Expression the Boolean function $F = A + \bar{B}C$ in a sum of minterms form.	6	L3	CO3
	b.	Express the Boolean function $F = xy + \bar{x}z$ in product of maxterms form.	6	L3	CO3
	c.	Design a Full adder circuit using two Half adders.	8	L3	CO3

		Module – 4			
Q.7	**a.**	Compare Embedded System with General computing system.	**7**	**L2**	**CO4**
	b.	Explain element of an embedded system with the help of a block diagram.	**8**	**L2**	**CO4**
	c.	Explain major application areas of Embedded System.	**5**	**L2**	**CO4**
		OR			
Q.8	**a.**	Compare Microprocessors and Microcontrollers.	**6**	**L2**	**CO4**
	b.	Compare RISC and CISC processors.	**6**	**L2**	**CO4**
	c.	Explain working of a 7 segment LED with necessary diagrams.	**8**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	Describe communication system with the help of a block diagram.	**8**	**L2**	**CO5**
	b.	Define Noise. Derive the expression for signal to Noise Ratio (SNR) in decibels (dB)	**7**	**L2**	**CO5**
	c.	What are advantages of Digital communication over Analog Communication	**5**	**L2**	**CO5**
		OR			
Q.10	**a.**	Explain Amplitude Modulation (AM) with necessary waveforms.	**7**	**L2**	**CO5**
	b.	What are different types Radio Wave propagation. Describe each type in detail.	**8**	**L2**	**CO5**
	c.	Describe various multiple access techniques used in communication systems.	**5**	**L2**	**CO5**

* * * * *

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Assignment -I

Department: Electronics & Communication			Name of the faculty: Nandini G R
Course Title: Introduction to Electronics & Communication			Course Code : BESCK104C
Semester : I	Section: A& B	Date of assignment:25/10/2023	Last date for submission:3/11/2023

Q.No.	QUESTIONS	Marks	CL	CO	PO
1	Draw the block diagram of DC power supply and explain the individual blocks.	10	U	22C104.1	1,6
2	With a neat circuit diagram and waveform. Explain the working operation of a half wave rectifier.	10	U	22C104.1	1,2,3 ,6
3	With a neat circuit diagram and waveform. Explain the working operation of a full wave rectifier.	10	U	22C104.1	1,2,3 ,6
4	With a neat circuit diagram and waveform. Explain the working operation of a full wave bridge rectifier.	10	U	22C104.1	1,2,3 ,6
5	Draw the circuit diagram of voltage regulation and explain the operation.	10	U	22C104.1	1,2,3 ,5
6	Describe the working of a capacitor filter for a half wave rectifier with a neat circuit diagram and necessary waveforms.	10	U	22C104.1	2,5
7	Describe the working of a capacitor filter for a full wave rectifier with a neat circuit diagram and necessary waveforms.	10	U	22C104.1	2,5
8	a)An amplifier produces an output voltage of 2V for an input of 50mV. If the input and output currents in this condition are 4mA and 200mA respectively. Find: i) The voltage gain ii) The current gain iii) The power gain. b) A 5V zener diode has a maximum rated power dissipation of 500 mW. If the diode is to be used in a simple regulator circuit to supply a regulated 5V to a load having a resistance of 400 Ω, determine a suitable value of series resistor for operation in conjunction with a supply of 9V.	10	Ap	22C104.1	1,2,5 ,6 1,2,3 ,5
9	Discuss briefly a negative feedback amplifier with block diagram and Derive for Voltage gain.	10	U	22C104.1	1,2,3 ,5
10	Draw the circuit diagram of voltage doubler and voltage tripler and explain the working operation.	10	U	22C104.1	1,2,5 ,6

(CL) Cognitive Level

(R): Remembering, (U): Understanding, (Ap): Apply, (A):Analysis, (E): Evaluation, (C): Creation.

COURSE OUTCOMES (COs) COVERED

CO1: Describe the concepts of electronic circuits encompassing power supplies, amplifiers and oscillators

Academic Coordinator
(Prof.Nandini G R)

H.O.D
(Dr.Siddesh K.B)

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Assignment -II

Department: Electronics & Communication Engineering			**Name of the faculty: Nandini G R**
Course Title: Introduction to Electronics & Communication			**Course Code :BESCK104C**
Semester :I	**Section: A& B**	**Date of assignment:01/12/2023**	**Last date for submission:15/12/2023**

Q.No.	QUESTIONS	Marks	CL	CO	PO
1	What is Op-Amp? What are the characteristics of an ideal operational amplifier?	05	U	22C104.2	1,2,3,5
2	Explain the following terms with reference to Operational Amplifiers. (i) Open loop voltage gain (ii) Closed loop voltage gain (iii) Input resistance (iv) Output resistance (v) Input offset voltage (vi) Slew rate	05	U	22C104.2	1,2, 3,6
3	Describe the three basic configurations for operational amplifier.	05	U	22C104.2	1,2, 3,6
4	Explain a differentiator circuit with waveforms and circuit diagrams.	05	U	22C104.2	1,3, 5,6
5	Explain a integrator circuit with waveforms and circuit diagrams.	05	U	22C104.2	1,3, 5,6
6	Sketch the circuits of each of the following based on the use of Op-Amp along with input and output waveforms: (i)Summing Amplifier (ii) Voltage follower (iii) Comparator	05	U	22C104.2	1,3, 5,6
7	Describe wein bridge oscillator with circuit diagram and formulas for frequency of oscillations.	05	U	22C104.2	1,2, 3,5
8	Explain the operation of three- stage ladder RC Network Oscillator with neat circuit diagram.	05	U	22C104.2	1,2, 3,5
9	Determine the frequency of oscillations of a 3-stage ladder network oscillator in which C=10nF and R= 10kΩ.	05	Ap	22C104.2	1,2, 3,5
10	Explain the Barkhausen criteria for Oscillations. In wein bridge oscillator if C1=C2=100nF, determine the frequency of oscillations when R1=R2=1kΩ	05	Ap	22C104.2	1,2, 3,5
11	Explain the operation of Single stage Astable multivibrator with its circuit diagram.	05	U	22C104.2	1,2, 3,5
12	Convert the following: (i) $(1AD.E0)_{16}=(?)_{10}$ (ii) $(37.625)_{10}=(?)_{2}$ (iii) $(110100111001.110)_{2}=(?)_{8}$	05	Ap	22C104.3	1,2, 3,5

Assignment -II

	(iv) $(345.AB)_{16}=(?)_2$ (v) $(1101.1)_2=(\ ?\ )_{10}$ (vi) $(186.75)_{10}=(\ ?\ )_2$ (vii) $(0110110111.1101)_2=(\ ?\ )_8$ (viii) $(64.73)_8=(\ ?\ )_{16}$ (ix) $(AC.DB)_{16}=(\ ?\ )_2$ (x) $(426.21)_8=(\ ?\ )_{10}$				
13	Perform the following operations: (i) 1101-0101 using 1's complement method. (ii) 0110-0010 using 2's complement method. (iii) 924-126 using 9's complement method. (iv) 265-424 using 10's complement method. (v) 1010100-1000100 using 1's complement method. (vi) 1010100-1000100 using 2's complement method. (vii) 4456-34234 using 9's complement method. (viii) 4456-34234 using 10's complement method.	05	Ap	22C104.3	1,2, 3,5
14	State and prove De-Morgan's theorems with its truth table.	05	U	22C104.3	1,2, 3,9
15	Implement full adder circuit with its truth table and write the expressions for sum and carry.	05	Ap	22C104.3	1,3, 5,9
16	Design a Half Adder circuit with necessary logic diagram and expressions.	05	Ap	22C104.3	1,3, 5,9
17	Design a Full adder circuit using two Half adders.	05	Ap	22C104.3	1,3, 5,9
18	Express the Boolean function F= A+ $\bar{B}$C in a sum of minterms form.	05	Ap	22C104.3	1,2, 3,5, 9
19	Express the Boolean function F= XY + $\bar{X}$ Z in a product of maxterms form.	05	Ap	22C104.3	1,3, 5,9
20	Simplify the following expressions using Boolean algebra: (i) $\bar{A}$BC + AB$\bar{C}$ +AB (ii) $A + BC + B$	05	Ap	22C104.3	1,3, 5,9

(CL) Cognitive Level

(R): Remembering, **(U)**: Understanding, **(Ap)**: Apply, **(A)**:Analysis, **(E)**: Evaluation, **(C)**: Creation.

COURSE OUTCOMES (COs) COVERED

22C104.1: Describe the concepts of electronic circuits encompassing power supplies and amplifiers .

22C104.2: Describe the concepts of Oscillators and Operational amplifiers.

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Assignment -II

22C104.3: Develop competence knowledge to construct basic digital circuits by make use of basic gate and its function.

22C104.4: Discuss the characteristics and technological advances of embedded systems.

22C104.5 Explain the different modes of communication from wired to wireless and the computing involved

Academic Coordinator
(Prof.Nandini G R)

H.O.D
(Dr.Siddesh K.B)

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Assignment 1 submission report		
Name of the Faculty: NANDINI G R	**Department: E&CE**	
Subject Name: Introduction to Electronics and Communication	**Semester:1st**	**Section: A**
Subject Code: BESCK104C	**Date of assignment:25/10/2023**	**Last date for submission:3/11/2023**

Sl No	BRANCH	NAMEOFTHESTUDENT	Marks	Signature
1.	CS	ABHINAIK N	10	
2.	CS	ABHISHEK L	10	
3.	CS	AISHA ABDUL SHUKOOR	10	
4.	CS	AKARSHA SAJJAN B	10	
5.	CS	AKASH G	10	
6.	CS	AMITH PATIL	10	
7.	CS	AMITH V	10	
8.	CS	AMRUTHA C M	10	
9.	CS	ANKITHA J	10	
10.	CS	ANUSHAR H	10	
11.	CS	ANUSHREEP M	10	
12.	CS	ARPITHA R	10	
13.	CS	BHAVANASHREE S	10	
14.	CS	CHAITRA B	10	
15.	CS	CHAITRA JAGADISH BADEGONDRA	10	
16.	CS	CHAITRA SURESH ARIKATTE	10	
17.	CS	CHANDANA S R	10	
18.	CS	CHANDANA V	10	
19.	CS	CHIDANANDA G	10	
20.	CS	CHINMAYEE U	10	
21.	CS	CHINMAYI M K	10	
22.	CS	DARSHAN B S	10	
23.	CS	DARSHAN G P	10	
24.	CS	DARSHITHA G P	10	
25.	CS	DHANUSH H	10	
26.	CS	DILIP M P	10	
27.	CS	DIVYA U	10	
28.	CS	G R GOWRI	10	
29.	CS	GANESH C Y S	10	
30.	CS	GANESH M M	10	
31.	CS	GHOUSIYA FATHIMA A	10	
32.	CS	GIRISH KUMAR M	10	
33.	CS	GIRISH PARAGOND KAMATAGI	10	
34.	CS	GULAM HUSSAIN	10	
35.	CS	HRUTHIK S	10	

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36.	CS	JAYANTH S P	10	
37.	CS	JEEVAN R	10	
38.	CS	K S KISHAN	10	
39.	CS	KARTHIK E HALAGERI	10	
40.	CS	KARTHIK J	10	
41.	CS	KAVANA K	10	
42.	CS	KIRAN JADADARI	10	
43.	CS	KUSUMA M	10	
44.	CS	LAKSHMANA N	10	
45.	CS	MADHURA G M	10	
46.	CS	MANUSHREE M	10	
47.	CS	MEGHA MANJAPPA MOGALI	10	
48.	CS	MEGHANA A B	10	
49.	CS	MEGHANA G S	10	
50.	CS	MINAL R SGOWDA	10	
51.	CS	MOHAMAD MUTHAWAKAL G	10	
52.	CS	MOHAMED GHOUSE	10	
53.	CS	MOHAMMED SHAFIQ	10	
54.	CS	MOHAMMED SHREYAN	10	
55.	CS	MUBARAK PASHA	10	
56.	CS	MUTHURAJ J R	10	
57.	CS	NAGARAJ G R	10	
58.	CS	NANDINI G R	10	
59.	CS	PRAVALIKA	10	
60.	CS	T M RITHIN	10	
61.	CS	V TEJASWINI	10	
62.	CS	YUVARAJ D	10	
63.	CS	SUHAFATHIMAM J	10	

Signature of the faculty

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Assignment 1 submission report		
Name of the Faculty: NANDINI G R	**Department: E&CE**	
Subject Name: Introduction to Electronics and Communication	**Semester:1st**	**Section: B**
Subject Code: BESCK104C	**Date of assignment:25/10/2023**	**Last date for submission:03/11/2023**

Sl No	BRANCH	NAMEOFTHESTUDENT	Marks	Signature
1.	CS	ASHWINI HIREGOUDRU	10	
2.	CS	HARISH P	10	
3.	CS	JAYANTH KUMAR	10	
4.	CS	MOHAMMED ANAS M	10	
5.	CS	NAVEEN V	10	
6.	CS	NIKHIL G	10	
7.	CS	NIRMALA BASAVARAJ MALI	10	
8.	CS	NIRMITHA P	10	
9.	CS	NIRUP A	10	
10.	CS	NITHYA S	10	
11.	CS	PALADUGU TEJASWINI	10	
12.	CS	POORNIMA RAJ N	10	
13.	CS	PRANAV H ORIGANTI	10	
14.	CS	PREETHI V M	10	
15.	CS	PRIYANKA P H	10	
16.	CS	PRUTHVI P	10	
17.	CS	R K SUMANTH	10	
18.	CS	RAHUL N	10	
19.	CS	RAKSHITHA H	10	
20.	CS	RAKSHITHA M H	10	
21.	CS	RAMYA V	10	
22.	CS	RAMYASHREE S S	10	
23.	CS	ROHITH RAJU GIDDAPPANAVAR	10	
24.	CS	RUMMAN AHAMED KHAN	10	
25.	CS	S HEMA	10	
26.	CS	SAHANA G S	10	
27.	CS	SANDEEPRAJ S N	10	
28.	CS	SHAHAJAN A R	10	
29.	CS	SHAMBHAVI G S	10	
30.	CS	SHASHANK K G	10	
31.	CS	SHREYAS B ACHARYA	10	
32.	CS	SHREYAS RAJ V B	10	
33.	CS	SIDDESH D S	10	
34.	CS	SINCHANA PATEL	10	
35.	CS	SIRISHA D	10	

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36.	CS	SOMESHA K	10	Somesha K
37.	CS	SPANDANA K P	10	Spandana K P
38.	CS	SUCHITRA H	10	Suchitra H
39.	CS	SUMERIYA N	10	Sumeriya N
40.	CS	SUSHMITHA H	10	
41.	CS	SWATI SHANMUKHA SURAGIMATH	10	
42.	CS	SYED ABDULLA S	10	Syed
43.	CS	SYED AQEEB AHAMAD	10	
44.	CS	SYEDA NAAZ Z	10	Naaz
45.	CS	T RAKSHITHA	10	
46.	CS	TAJ MOHAMMED WASI UR RAHAMAN	10	
47.	CS	TARUN KUMAR S	10	Tarun-S
48.	CS	THARA R	10	Thara R
49.	CS	UMMAR FAROOKH	10	
50.	CS	VAISHNAVI R	10	
51.	CS	VAMSHI M R	10	
52.	CS	VAMSHI R	10	
53.	CS	VIDYASHREE R	10	
54.	CS	VIKAS	10	
55.	CS	VIKAS R RATHOD	10	
56.	CS	YASHASWINI L M	10	
57.	CS	YASHASWINI S J	10	
58.	CS	ULLAS N	10	
59	CS	Supriya. G.N		Supriya. G.N

Signature of the faculty

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S. J. M INSTITUTE OF TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

P.B. No. 73,NH4 By-pass, Chitradurga -577502

Assignment-1

on

"INTRODUCTION TO ELECTRONICS AND COMMUNICATION"

(Subject Code: BESCK104C)

Submitted To

Prof. Nandini G R B.E., M.Tech.
Asst. Professor, Dept. of E&CE,
S.J.M.I.T, Chitradurga.

Name of the Student: Mohamad Muthawakkal G. **USN:**

Subject: Introduction to Electronics and Communication **Semester:** I

Subject Code: BESCK104C **Section: A**

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Assignments	Submission Date	Assignment Topics	Page No	Faculty Signature	Remarks
Assignment-1	06/11/2023	Power Supplies and Amplifiers	16		Good
			Assignment Marks	10	

Faculty Signature

1. Draw the block diagram of DC power supply and explain the individual blocks.

Stepdown transformer:

It is a device that has two coil windings: primary and secondary used to convert a high AC voltage to required low AC voltage

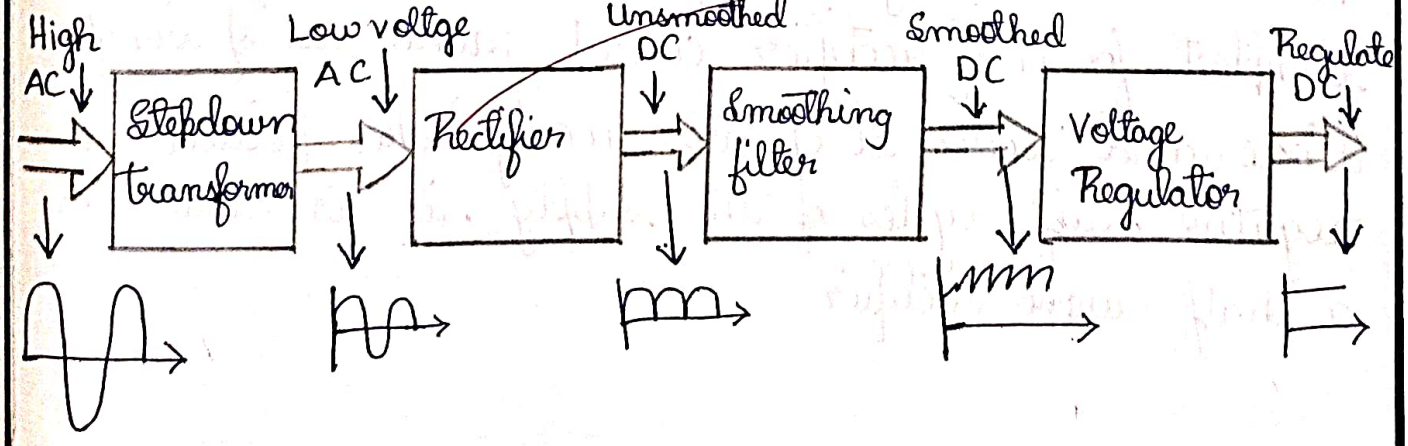
Rectifier:

It is a device has one or more diodes, converts secondary AC voltage to pulsating DC.

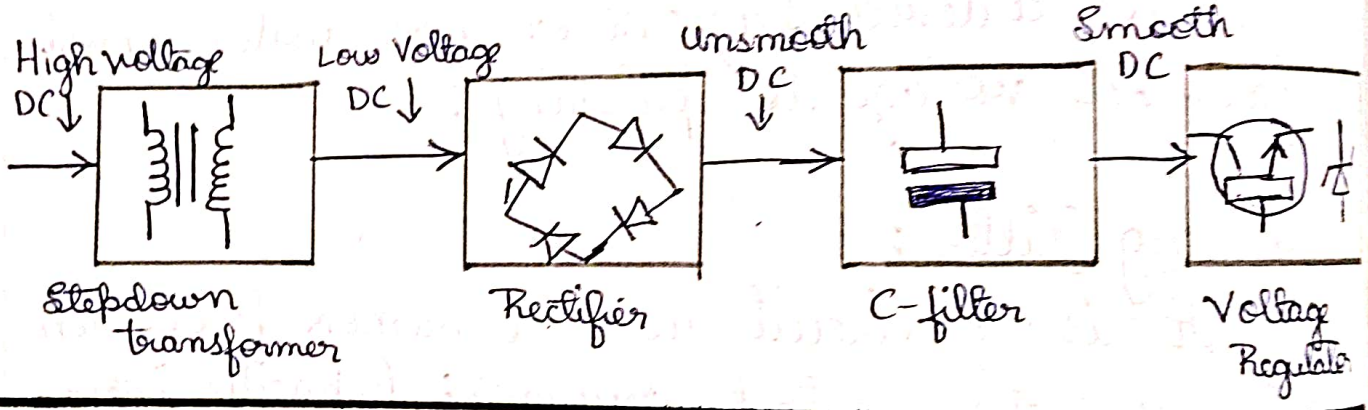
Smoothening Filter:

It is a circuit used to remove fluctuation present in rectifier output. Example: Capacitor filters, π filters, etc

Voltage Regulator: It is a circuit which provides constant DC output voltage irrespective of change in load current or changes in input voltages

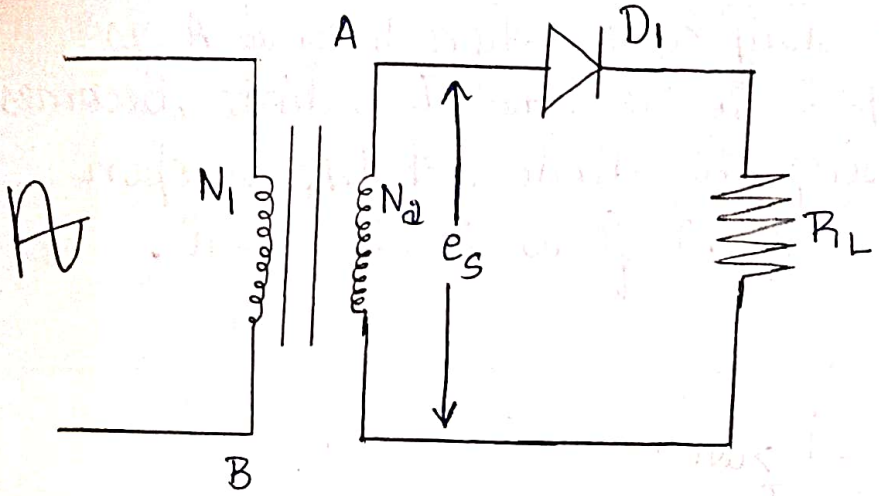


Step-down transformer is made of iron core, feds rectifiers. Rectifiers output is applied to high valu capacitor to minimize ripples. Capacitor filter charg as the rectifiers output voltages increases until its p value. When the voltage value reduces, it discharge gradually through the regulator. Finally, a series transistor regulator and zener diode provides a constant output DC voltage

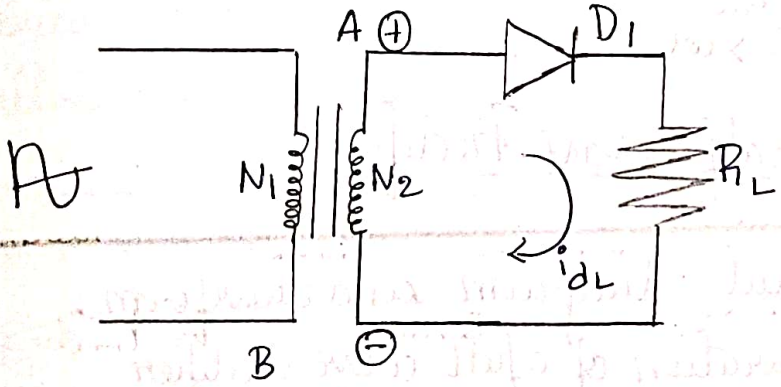


a. With neat circuit diagram and waveform. Explain the working operation of half wave rectifier

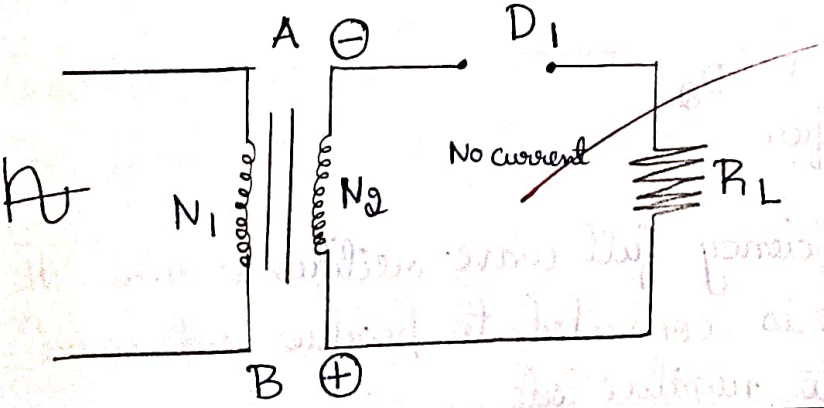
Semiconductor diodes are commonly used to convert AC to DC, they are referred to as rectifiers. The simplest form of rectifier circuit makes use of single diode and since it operates on only either positive or negative half-cycles of the supply, it is known as a half-wave rectifier



During positive half cycle



During positive half cycle terminal A become positive with respect to terminal B. The diode is forward biased and will efficiently behave liked a closed switch and the current flows in the circuit in the clockwise direction. This current is also flowing through the load resistor R_L



During negative half cycle when terminal A is negative with respect to terminal B, diode become reverse biased causing the diode act like an open switch. Hence no-current flows in the circuit.

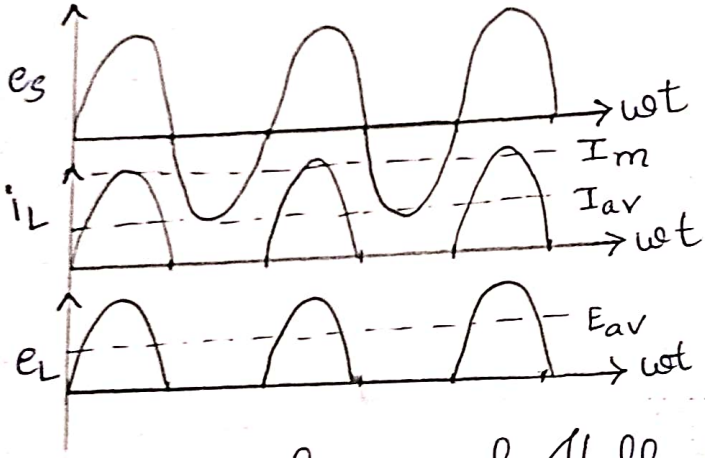


fig: Waveform of Half-Wave Rectifier

3. Write a neat circuit diagram and waveform. Explain the working operation of a full wave rectifier

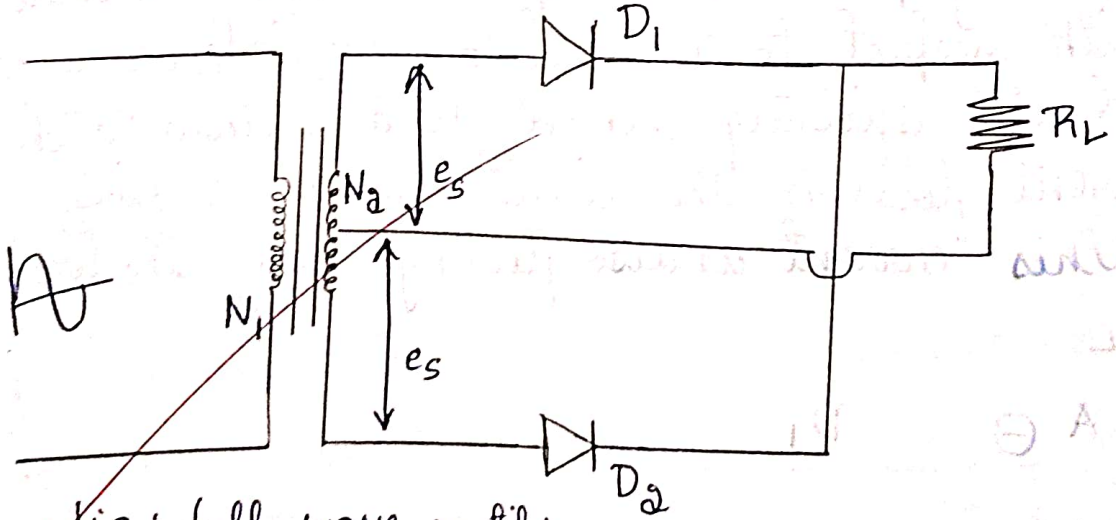
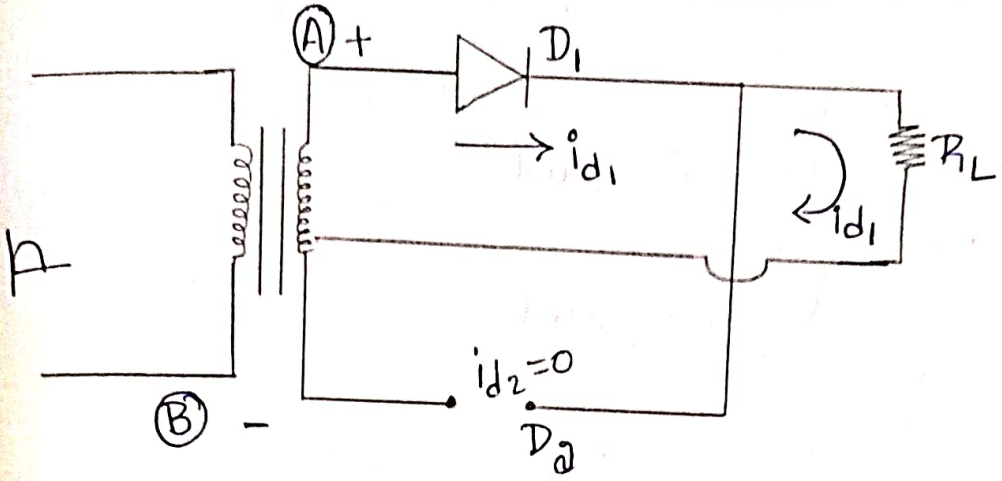
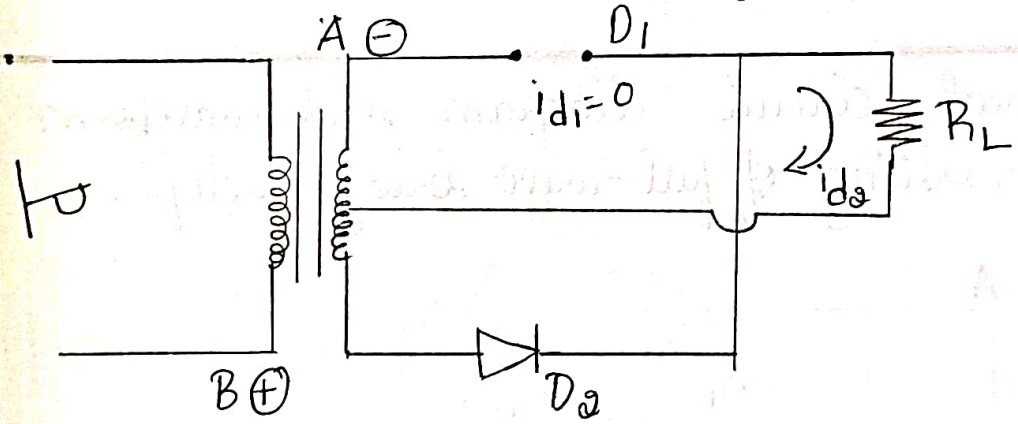


fig: full wave rectifier

To increase efficiency full wave rectifier is used. It contain two diode one is connected to positive side and another is connected to negative side

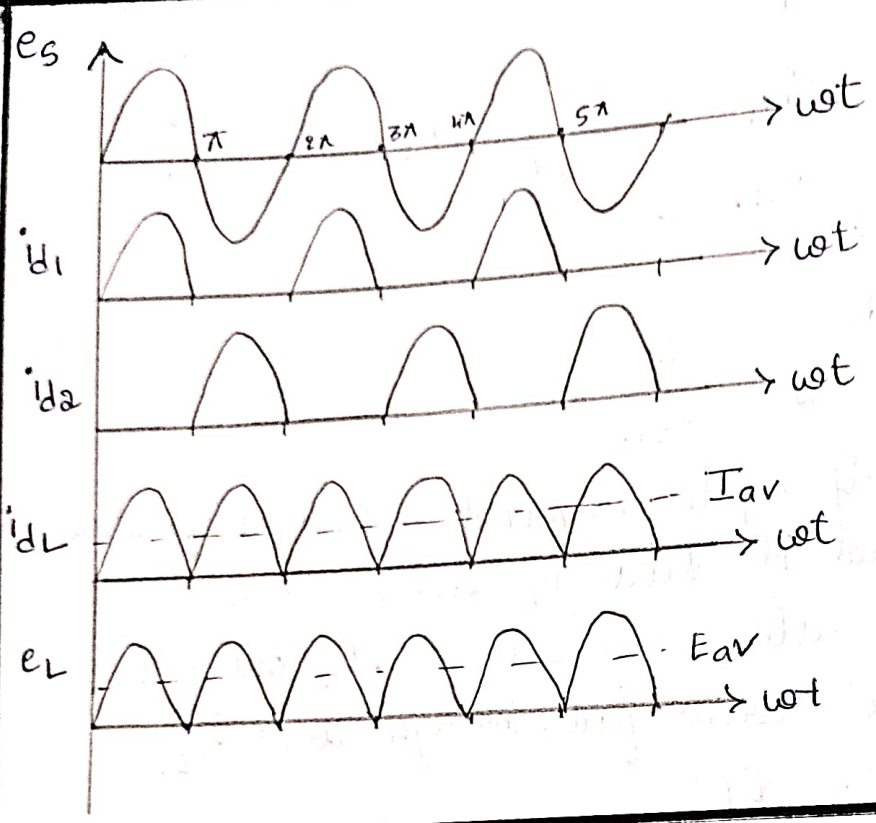


On positive half cycle terminal A become positive with respect to terminal B. Diode D_1 become forward bias and D_1 will allow conduction. D_2 will not allow conduction. The current flows through load R_L



On Negative half cycles, point B will be positive with respect to point A. Diode D_2 become forward bias and D_2 conduct current act as closed switch Diode D_1 does not conduct current. The current flows in clockwise direction which moves from load resistor R_L.

The total current $i_{dL} = i_{d1} + i_{d2}$



4. Write a neat circuit diagram and waveform Explain the working of full-wave bridge rectifier

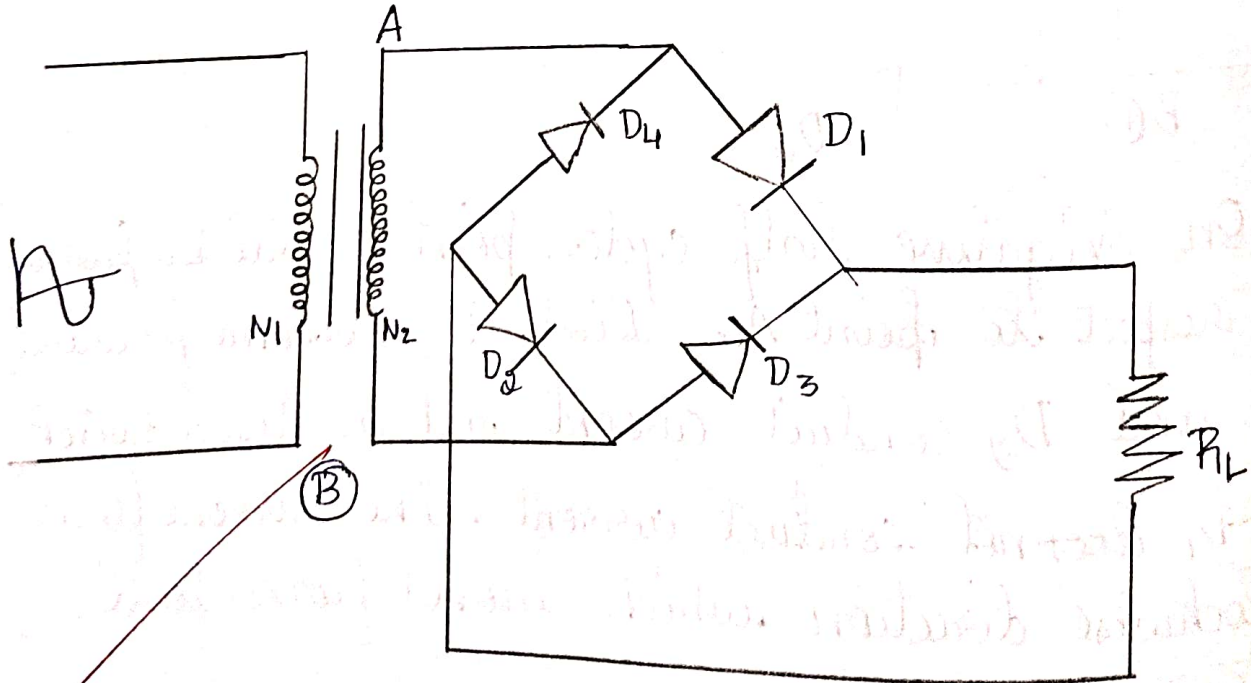
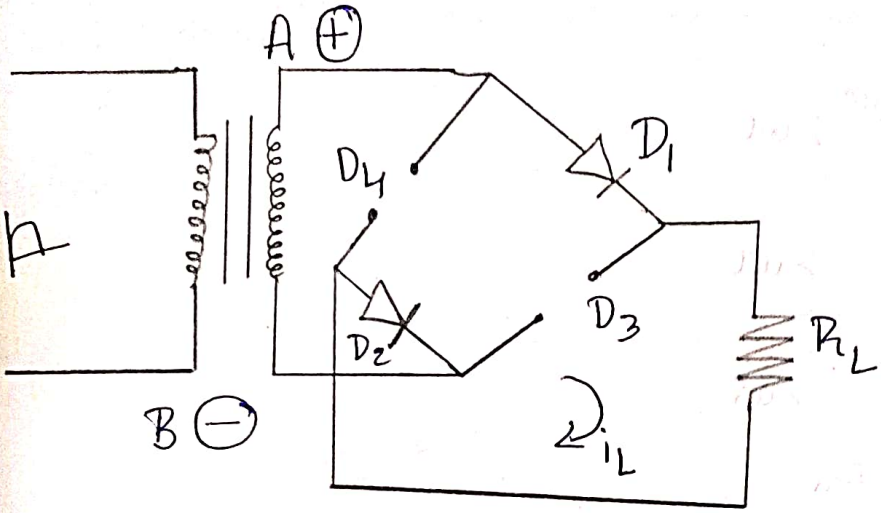
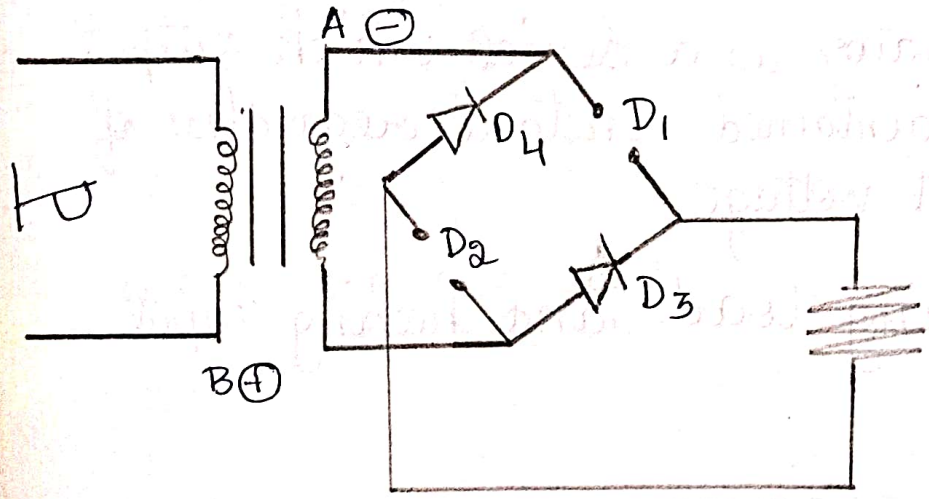


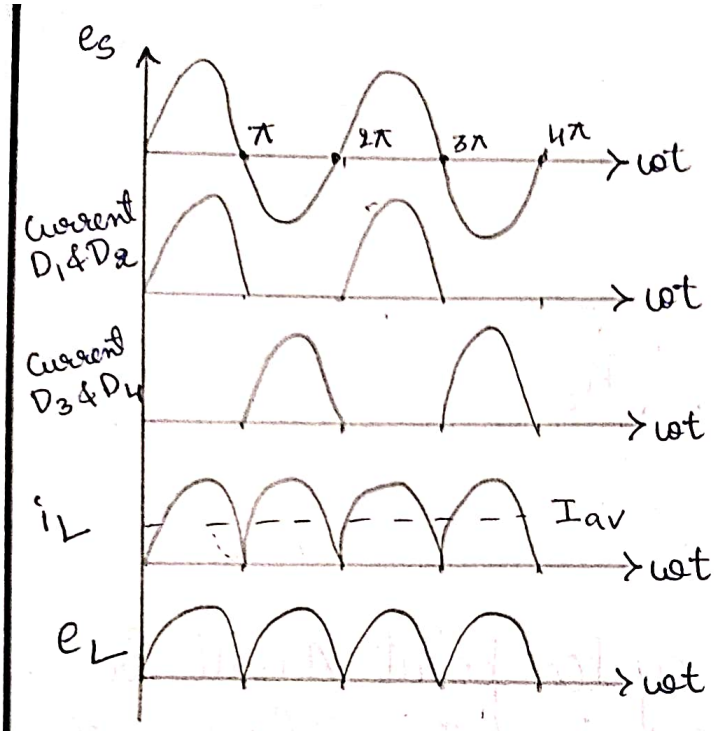
fig: full wave - bridge rectifier



On positive half cycles. point A will be positive with respect to terminal B. The current will be conduct at diode D_1 and D_2 while diode D_3 and D_4 will not allow conduction



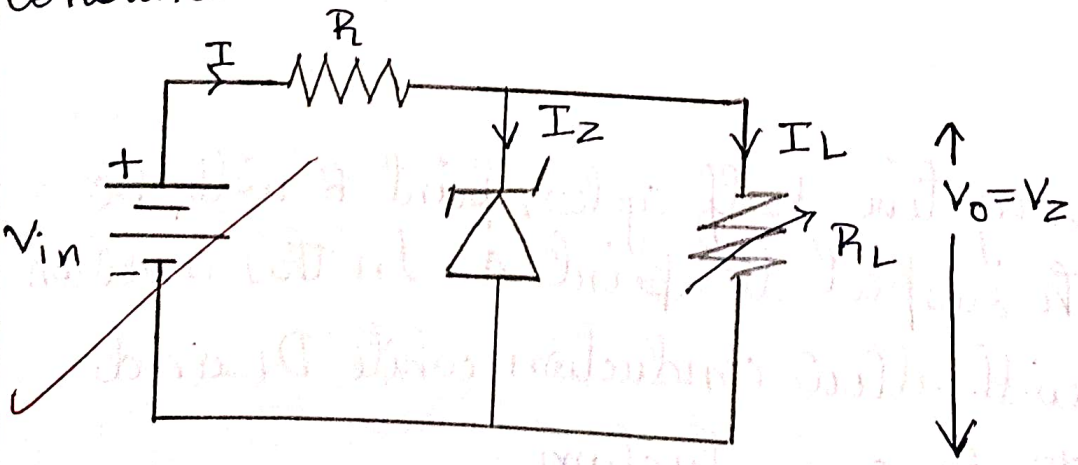
On negative half cycles, point B will be positive with respect to point A. In this condition D_3 and D_4 will allow conduction while D_1 and D_2 will not allow conduction



5. Draw the circuit diagram of voltage regulation and explain the operation

Voltage regulator is a device which output voltage is maintained constant regardless of change in input voltage.

Case 1: By varing load and keeping Input constant



The fig show zener regulator under varing load

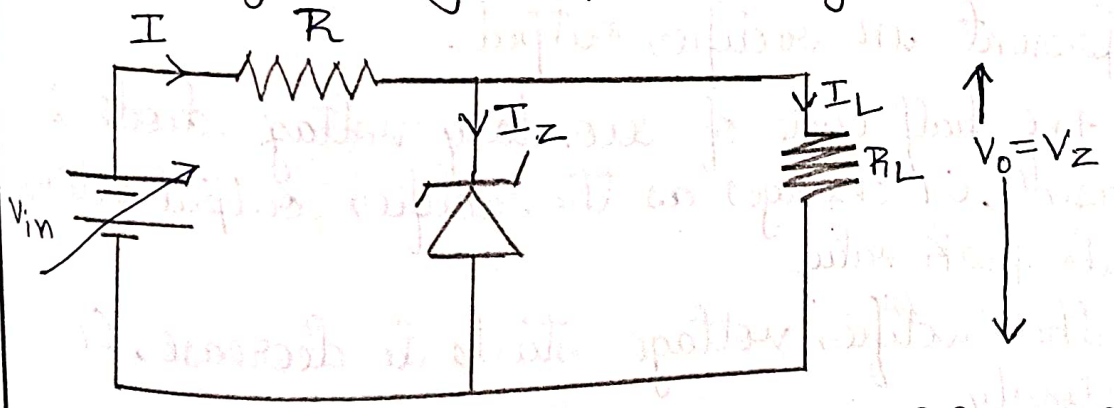
The input voltage is constant while the load resistor R_L is variable

- As V_{in} is constant and $V_o = V_z$ is constant

$$I = \frac{V_{in} - V_z}{R}$$, constant $I_L + I_z$

- Now if R_L decreases so I_L increase, to keep I constant I_z decreases. But as long as it is in between $I_{z\min}$ & $I_{z\max}$. Output voltage V_z will be constant
- Similarly if R_L increase so I_L decrease, to keep I constant I_z increases. But as long as it is in between $I_{z\min}$ & $I_{z\max}$. Output voltage V_o will be constant

Case 2: By varing Input voltage



This fig shows a zener regulator under varing input voltage condition

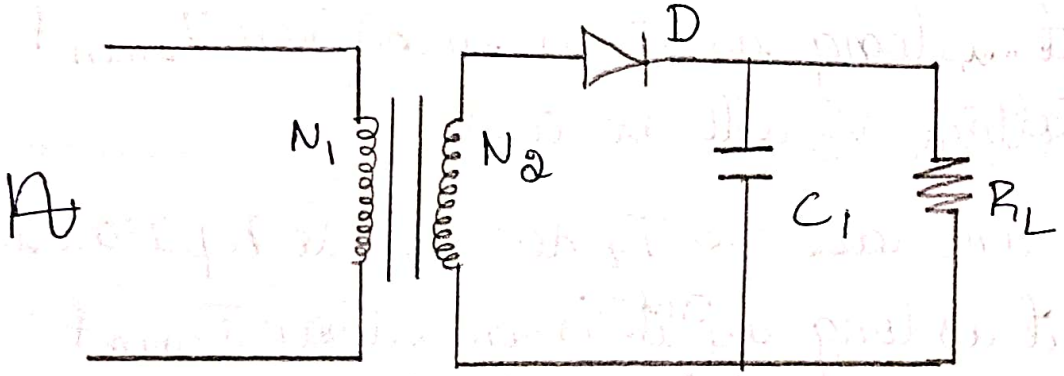
- It can be seen that the output is $V_o = V_z$ is constant

$\therefore I_L = \frac{V_o}{R_L} = \frac{V_z}{R_L}$ = constant

Now V_{in} increases, then the total current I increase. But I_L is constant as V_Z is constant. Hence the current I_Z increases to keep I_L constant

But as long as I_Z is between $I_{Z\,min}$ and $I_{Z\,max}$, the V_Z i.e, output voltage V_o is constant

6. Describe the working of a capacitor filter for a halfwave rectifier with a neat circuit diagram and necessary waveform



Smoothening circuit is a capacitor filter C1 connected in parallel to the load R_L. It is used to remove fluctuation present in rectifier output.

During +ve half cycle of secondary voltage, diode is forward biased, C1 charges as the rectifier output voltage increase to its peak value

When the rectifier voltage starts to decrease, C_1 discharges slowly

Charging time of $C_1 = R_{series} \times C_1$

Discharging time of $C_1 = R_L \times C_1$

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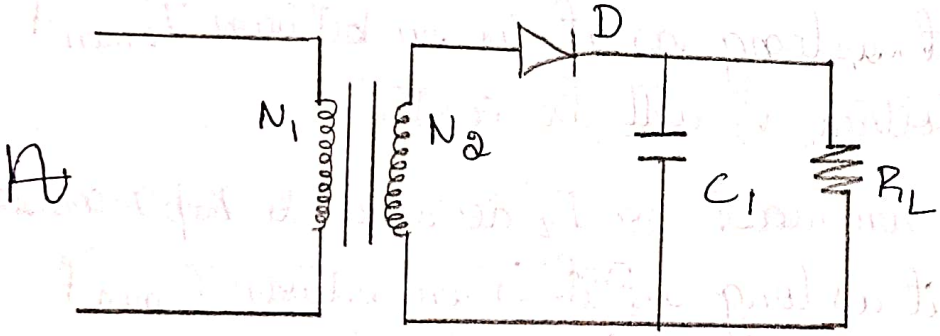

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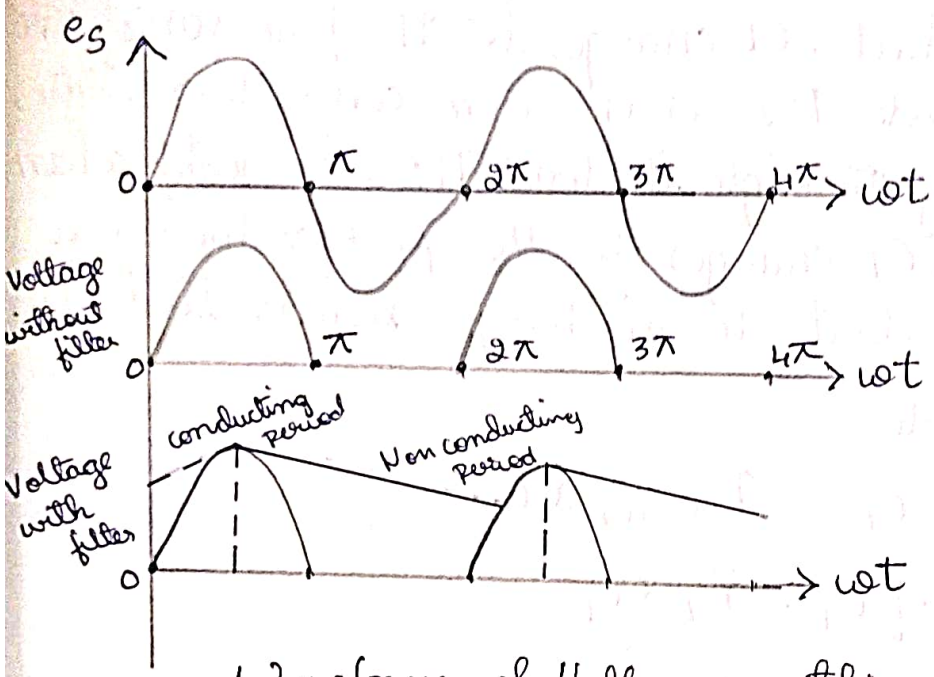
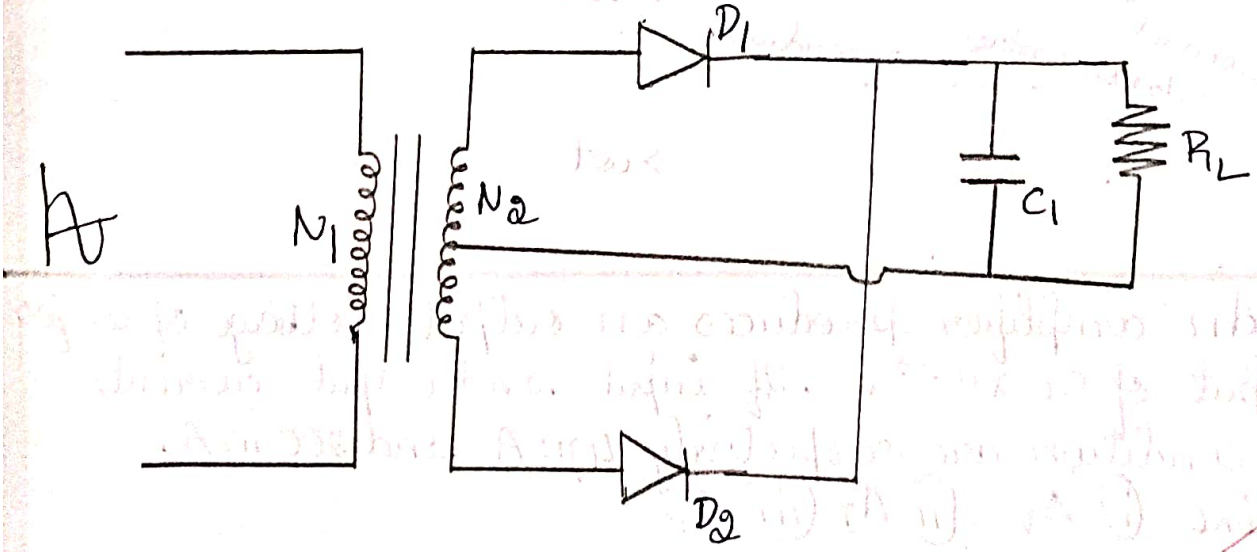


Waveform of Half wave rectifier with C-filter

7. Describe the working of capacitor filter of full wave rectifier with a neat circuit diagram and necessary waveform

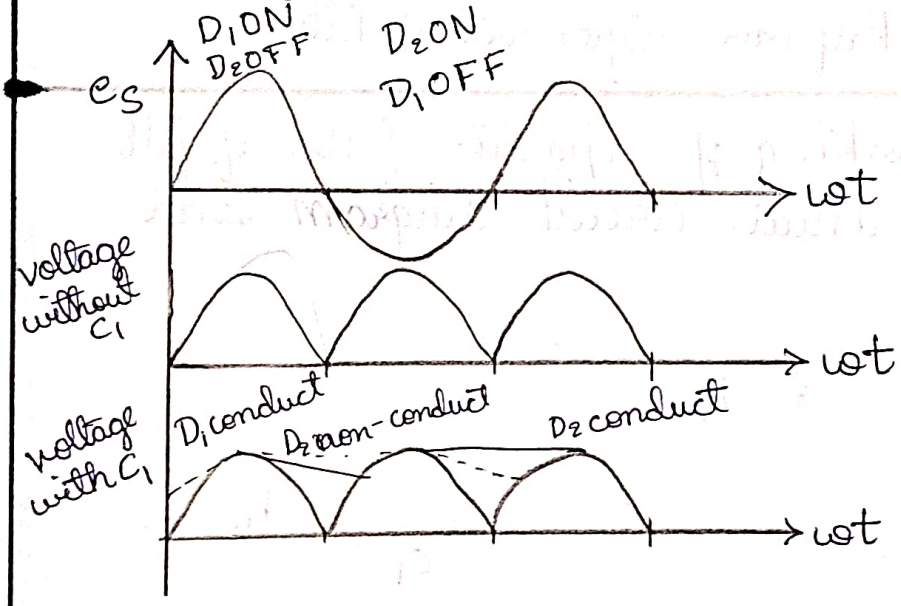


Two diodes D_1 and D_2 are used in this circuit. They feed a common load resistor R_L, with the help of centre tapped transformer

When diode D_1 conduct, C_1 charges to the peak vale of +ve half cycle. When diode D_2 is in non conducting state, C_1 discharges slowly through the load R_L. Similarly when diode D_2 conduct, C_1 charges to the peak value of -ve half cycle and C_1 starts to discharge during diode D_1 non-conducting state

Charging time of $C_1 = R_{series} \times C_1$

Discharging time of $C_1 = R_L \times C_1$



8.(a) An amplifier produces an output voltage of 2V for an input of 50×10^{-3} V. If input and output currents in this condition are respectively 4mA and 200mA, determine (i) A_V (ii) A_I (iii) A_P

(b) A 5V zener diode has a maximum rated power dispation of 500mW. If the diode is to be used in simple regulator circuit to supply a regulated 5V to a load having a resistance of 400Ω, determine a suitable value of series resistor for operation in conjunction with a supply of 9V

(a) (i) $A_V = \frac{V_{out}}{V_{in}} \Rightarrow \frac{2}{5\times10^{-3}}$

$A_V = 40$

(ii) $A_I = \frac{I_{out}}{I_{in}} \Rightarrow \frac{200\times10^{-3}}{4\times10^{-3}}$

$A_I = 50$

(iii) $A_P = \frac{P_{out}}{P_{in}} = \frac{2}{50\times10^{-3}} \times \frac{200\times10^{-3}}{4\times10^{-3}}$

$A_P = 2000$

(b) $R_{S_{min}} = \left(\frac{V_{in}V_Z - V_Z^2}{P_{Z_{max}}}\right)$

$R_{S_{min}} = \frac{9\times5 - 25}{500\times10^{-3}}$

$R_{S_{min}} = 40\,\Omega$

$R_{S_{max}} = R_L\left(\frac{V_{in}}{V_Z} - 1\right)$

$R_{S_{max}} = 400\left(\frac{9}{5} - 1\right)$

$R_{S_{max}} = 320\,\Omega$

Hence suitable value of R_S is between 40 Ω and 320 Ω

The value of R_S is roughly 150 Ω

9. Discuss briefly a negative feedback amplifier with block diagram and derive voltage gain

Practical amplifier use negative feedback in order to precisely control gain and improve bandwidth. The gain can be reduced to a manageable value by feeding back a small proportion of output. The feedback has the effect to reducing the overall gain of circuit, this form of the feedback is known as negative feedback.

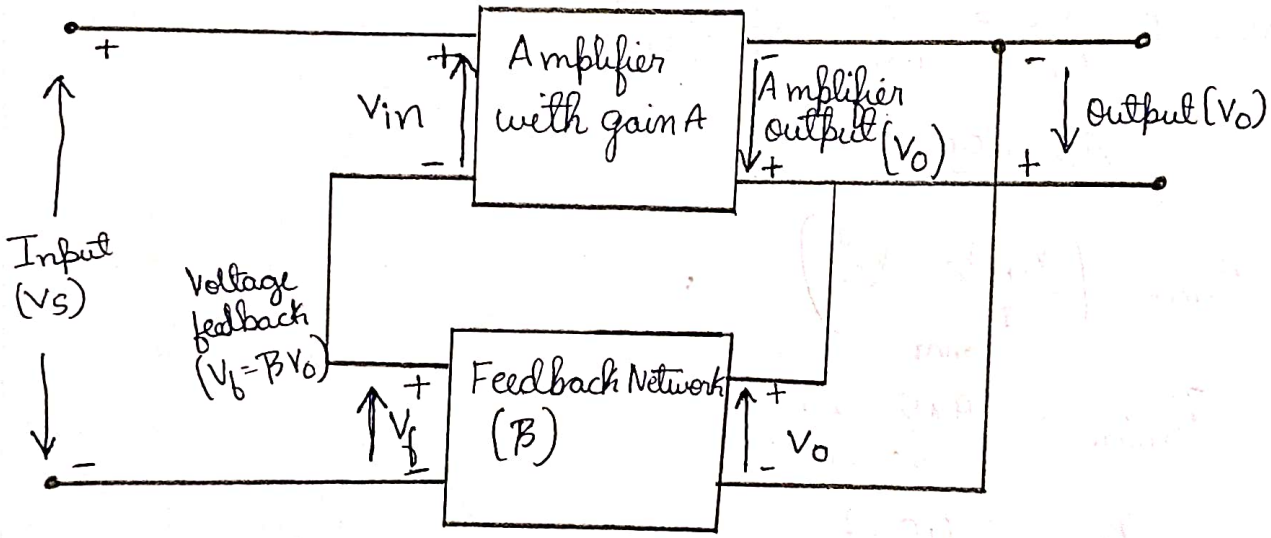


fig: Amplifier with negative feedback

Gain of Amplifier with feedback : $A_V = \frac{V_o}{V_s} \rightarrow (1)$

$$V_{in} = V_s - V_f$$

$$V_{in} = V_s - \beta V_o \rightarrow (2)$$

Gain of Amplifier without feedback : $A_V = \frac{V_o}{V_{in}}$

$$V_o = A V_{in}$$

$$V_o = A(V_s - \beta V_o)$$

$$V_o = AV_s - A\beta V_o$$

$$V_o + A\beta V_o = AV_s$$

$$V_o(1 + A\beta) = AV_s$$

$$\frac{V_o}{V_s} = \frac{A}{1 + A\beta}$$

$$A_v = \frac{A}{1 + A\beta}$$

10. Draw the circuit diagram of voltage doubler and tripler and explain the working operation

A voltage doubler using this technique. In this arrangement C_1 will charge to the positive peak secondary voltage while C_2 will charge to the negative peak secondary voltage. Since the output is taken from C_1 and C_2 connected in series the resulting output voltage is twice that produced by one diode alone

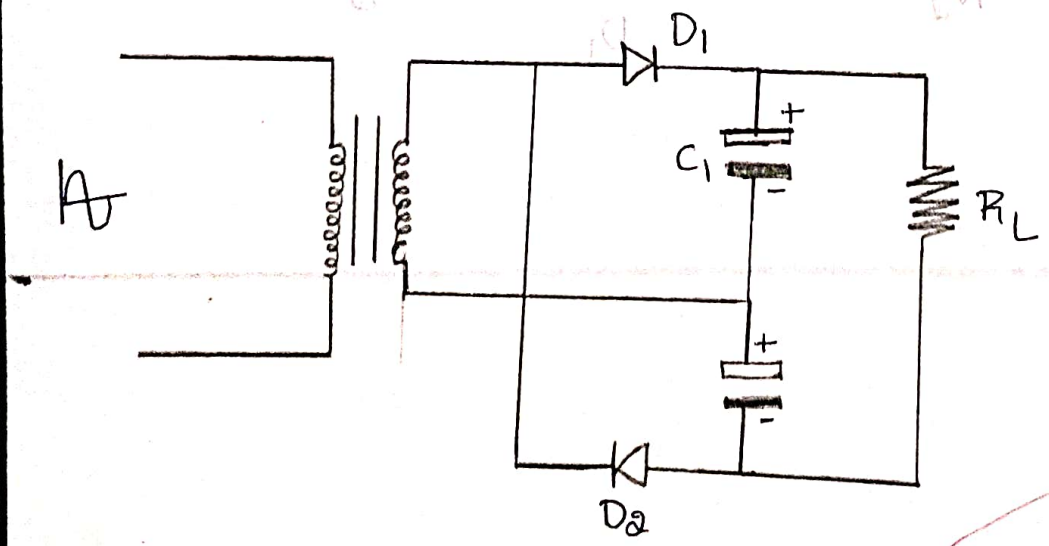
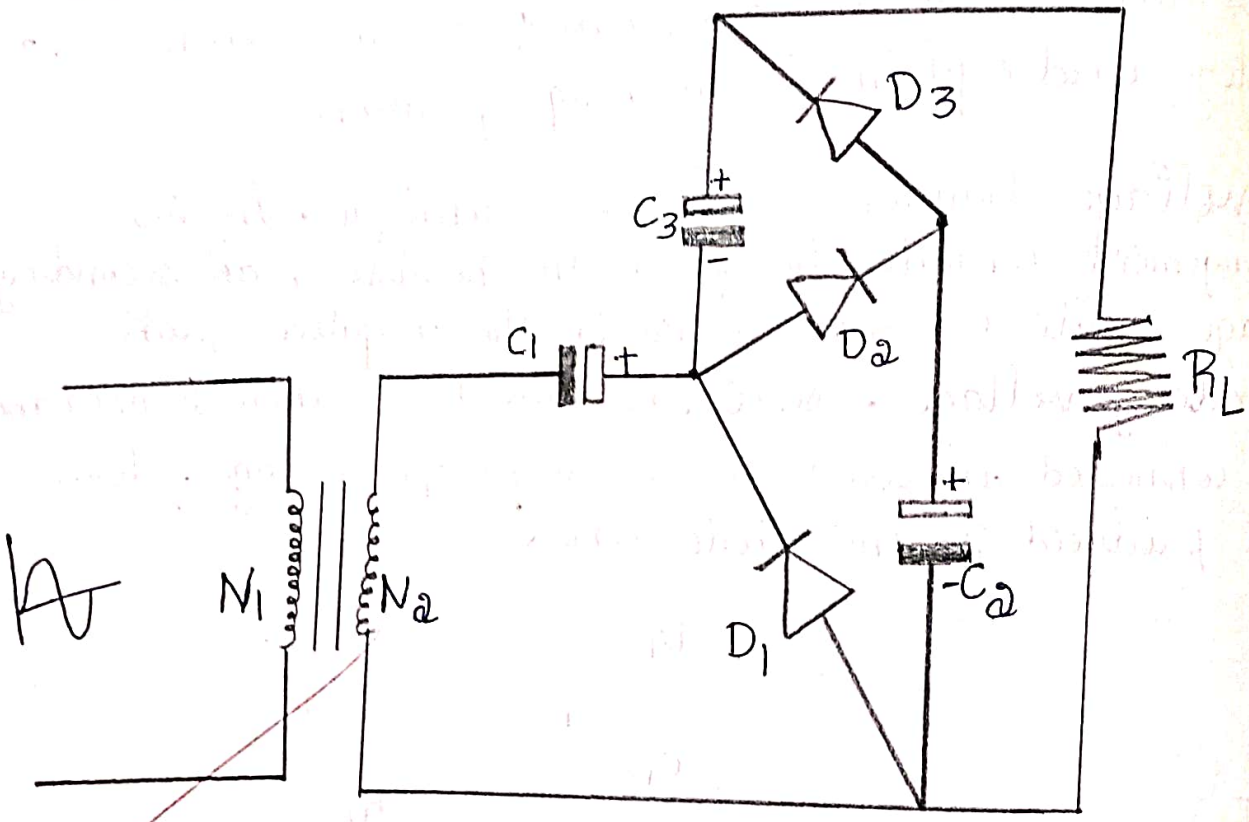


fig: Voltage doubler.

The voltage doubler can be extended to produce higher voltages using the cascade arrangement. Here C1 charges to the positive peak secondary voltage, while C2 and C3 charge to twice the positive peak of secondary voltage. The result is that the output voltage is the sum of the voltages across C1 and C3 which is three times the voltage that would be produced by a single diode



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NAAC Accredited with B++ Grade

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Sub: Introduction to Electronics and communication
Sub Code: BESCK104C
Max Marks: 15
Date: 29\12\2023

1. _____ are used to convert Alternating Current(AC) to Direct Current(DC)
   a. Transistor b.Inductors c. Diodes d. Transformers

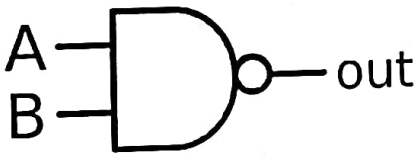
2. In reservoir/smoothing circuits of rectifiers_____is used as filter.
   a. Transistor b.Capacitor c. Diodes d. Transformers

3. A component that ensures a steady constant voltage supply through all operational conditions is called as_____
   a. Rectifier b.Amplifier c. Oscillator d. Voltage Regulators

4. The positive(+) input in an opamp is referred as_____
   a.Non Inverting Input b.Inverting Input c. Differential input d. Active input

5. Device that generates continuous train of pulses is called_____
   a.Astable Multivibrator b. Monostable Multivibrator c. Bistable Multivibrator d. Crystal Oscillator

6. The symbol shown below represents a_____



   a. AND gate b.NOR gate c. OR gate d. NAND gate

7. _____ is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN.
   a. Half Adder b.Full Adder c. Summing Amplifier d. Multiplexer

8. A _____ is a type of digital circuit using a cascade of flip-flops where the output of one flip-flop is connected to the input of the next
   a. Multiplexer b.Decoder c. Shift Register d. Counter

9. An electronic/electromechanical system designed to perform a Specific function and is a combination of both hardware and firmware is called as an_____

a. Communication system b.Embedded system c. Computing system d. Control system

10. A _____ is a silicon chip representing a central processing unit (CPU), which is capable of performing arithmetic as well as logical operations according to a pre-defined set of instructions, which is specific to the manufacturer.

a. Microprocessor b. Microcontroller c. ROM d. Both a & b

11. _____are devices which convert energy in the form into an equivalent electrical signal, or vice versa.

a. Decoders b. Flipflops c. Transducers d. Amplifiers

12._____ is a form of transducer device (mechanical or electrical) which converts signals to corresponding physical action (motion).

a. Actuator b.Sensor c. Multivibrator d. Transducer

13. When a PN junction is forward biased

a. Depletion region decreases

b. Minority carriers are not affected

c. Holes and Electrons moves away from the junction

d. All of the above

14. Modulation is done in .....

a. Receiver b.Transmitter c. Between Transmitter and Receiver d. None of the Above

15. Which option below lists the type of signal denoted by a sine wave?

a. Linear b.Digital c. Static. d. Analog

Academic Coordinator
(Prof.Nandini G R)

H.O.D
(Dr.Siddesh K.B)

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Quiz Attendance		
Name of the Faculty: NANDINI G R	**Department: E&CE**	
Subject Name: Introduction to Electronics and Communication	**Semester:1st**	**Section: A**
Subject Code: BESCK104C	**Date: 29/12/2023**	**Time: 10:11AM**

Sl No	BRANCH	NAMEOFTHESTUDENT	Marks	Signature
1.	CS	ABHINAIK N	13	
2.	CS	ABHISHEK L	14	
3.	CS	AISHA ABDUL SHUKOOR	15	
4.	CS	AKARSHA SAJJAN B	15	
5.	CS	AKASH G	15	
6.	CS	AMITH PATIL	15	
7.	CS	AMITH V	15	
8.	CS	AMRUTHA C M	15	
9.	CS	ANKITHA J	15	
10.	CS	ANUSHAR H	15	
11.	CS	ANUSHREEP M	15	
12.	CS	ARPITHA R	15	
13.	CS	BHAVANASHREE S	14	
14.	CS	CHAITRA B	15	
15.	CS	CHAITRA JAGADISH BADEGONDRA	15	
16.	CS	CHAITRA SURESH ARIKATTE	14	
17.	CS	CHANDANA S R	15	
18.	CS	CHANDANA V	14	
19.	CS	CHIDANANDA G	15	
20.	CS	CHINMAYEE U	14	
21.	CS	CHINMAYI M K	14	
22.	CS	DARSHAN B S	14	
23.	CS	DARSHAN G P	14	
24.	CS	DARSHITHA G P	15	
25.	CS	DHANUSH H	14	
26.	CS	DILIP M P	15	
27.	CS	DIVYA U	15	
28.	CS	G R GOWRI	14	
29.	CS	GANESH C Y S	14	
30.	CS	GANESH M M	14	
31.	CS	GHOUSIYA FATHIMA A	14	
32.	CS	GIRISHKUMARM	15	
33.	CS	GIRISHPARAGONDKAMATAGI	15	
34.	CS	GULAM HUSSAIN	15	
35.	CS	HRUTHIK S	15	

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36.	CS	JAYANTH S P	15	
37.	CS	JEEVAN R	15	
38.	CS	K S KISHAN	15	K.S. Kishan
39.	CS	KARTHIK E HALAGERI	14	
40.	CS	KARTHIK J	15	
41.	CS	KAVANA K	15	Kavana. K
42.	CS	KIRAN JADADARI	14	
43.	CS	KUSUMA M	15	Kusuma. M
44.	CS	LAKSHMANA N	14	Laxman
45.	CS	MADHURA G M	14	Madhura G.M
46.	CS	MANUSHREE M	15	Manushree. M
47.	CS	MEGHA MANJAPPAMOGALI	15	
48.	CS	MEGHANA A B	15	Meghana. A.B
49.	CS	MEGHANA G S	15	Meghana. G.S.
50.	CS	MINAL R SGOWDA	15	Minal. R.S. Gowda
51.	CS	MOHAMAD MUTHAWAKAL G	15	Muthakal.
52.	CS	MOHAMED GHOUSE	15	Md Ghouse
53.	CS	MOHAMMED SHAFIQ	15	
54.	CS	MOHAMMED SHREYAN	15	Md Shreyan
55.	CS	MUBARAK PASHA	15	
56.	CS	MUTHURAJ J R	15	Muthu Raj
57.	CS	NAGARAJ G R	15	Nagaraj G.R
58.	CS	NANDINI G R	15	Nandini
59.	CS	PRAVALIKA	15	Pravalika.
60.	CS	T M RITHIN	15	
61.	CS	V TEJASWINI	15	V. Tejaswini
62.	CS	YUVARAJ D	14	Yuvaraj. D.
63.	CS	SUHAFATHIMAM J	15	Suhafathima. J

Total Number of Students Present:	63
Number of Students Absent:	00
Total Number of Students:	63
Name & Signature of Invigilator	
Name & Signature of Subject In-Charge	

Signature of the faculty

Signature of the H.O.D